



# STK14C68

## CMOS nvSRAM

### High Performance

### 8K x 8 Nonvolatile Static RAM

PRELIMINARY

2

## FEATURES

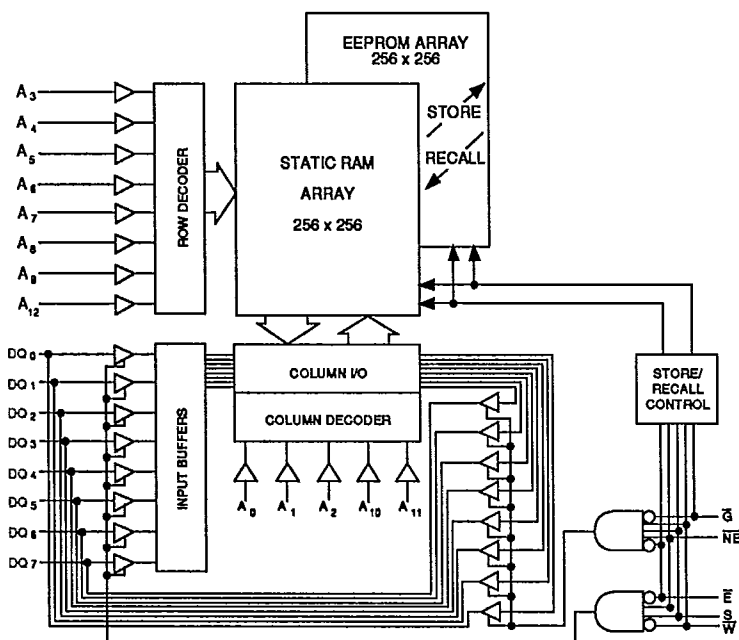
- 25, 30, 35 and 45ns Access Times
- 12, 15, 20 and 25ns Output Enable Access
- Unlimited Read and Write to SRAM
- Hardware *STORE* Initiation
- Automatic *STORE* Timing
- $10^4$  or  $10^5$  *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Hardware *RECALL* Initiation
- Unlimited *RECALL* cycles from EEPROM
- Single  $5V \pm 10\%$  Operation
- Commercial and Industrial Temperatures
- Available in multiple standard packages
- Chip Select and Chip Enable Pins

## DESCRIPTION

The Simtek STK14C68 is a fast static RAM (25, 30, 35, and 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (*STORE*), or from the EEPROM to the SRAM (*RECALL*) using the  $\overline{NE}$  pin. It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

The STK14C68 features industry standard pinout for nonvolatile RAMs in a 28-pin 300 mil plastic or ceramic DIP, and 28-pin SOIC.

## LOGIC BLOCK DIAGRAM



## PIN CONFIGURATIONS



28 - 350 SOIC  
28 - 300 FDIP  
28 - 300 CDIP

## PIN NAMES

$A_0 - A_{12}$	Address Inputs
W	Write Enable
$DQ_0 - DQ_7$	Data In/Out
E	Chip Enable
$\overline{G}$	Output Enable
NE	Nonvolatile Enable
S	Chip Select
$V_{CC}$	Power (+5V)
$V_{SS}$	Ground

## STK14C68

ABSOLUTE MAXIMUM RATINGS<sup>a</sup>

Voltage on typical input relative to $V_{SS}$ .....	-0.6V to 7.0V
Voltage on $DQ_{0-7}$ and $\bar{Q}$ .....	-0.5V to ( $V_{CC}+0.5V$ )
Temperature under bias.....	-55°C to 125°C
Storage temperature.....	-65°C to 150°C
Power dissipation.....	.1W
DC output current.....	.15mA

(One output at a time, one second duration)

**Note a:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC CHARACTERISTICS

 $(V_{CC} = 5.0V \pm 10\%)$ 

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
$I_{CC1}^b$	Average $V_{CC}$ Current		85		95	mA	$t_{AVAV} = 25ns$
			80		85	mA	$t_{AVAV} = 30ns$
			75		80	mA	$t_{AVAV} = 35ns$
			65		75	mA	$t_{AVAV} = 45ns$
$I_{CC2}^d$	Average $V_{CC}$ Current during STORE cycle		50		50	mA	$E \geq (V_{CC} - 0.2V)$ or $S \leq (V_{SS} + 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
$I_{SB1}^c$	Average $V_{CC}$ Current (Standby, Cycling TTL Input Levels)		30		34	mA	$t_{AVAV} = 25ns$
			27		30	mA	$t_{AVAV} = 30ns$
			23		27	mA	$t_{AVAV} = 35ns$
			20		23	mA	$t_{AVAV} = 45ns$
						$E \geq V_{IH}$ or $S < V_{IL}$ ; all others cycling	
$I_{SB2}^c$	Average $V_{CC}$ Current (Standby, Stable CMOS Input Levels)		1		1	mA	$E \geq (V_{CC} - 0.2V)$ or $S \leq (V_{SS} + 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
$I_{LK}$	Input Leakage Current (Any Input)		$\pm 1$		$\pm 1$	$\mu A$	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to $V_{CC}$
$I_{OLK}$	Off State Output Leakage Current		$\pm 5$		$\pm 5$	$\mu A$	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to $V_{CC}$
$V_{IH}$	Input Logic "1" Voltage	2.2	$V_{CC}+5$	2.2	$V_{CC}+5$	V	All Inputs
$V_{IL}$	Input Logic "0" Voltage	$V_{SS}-5$	0.8	$V_{SS}-5$	0.8	V	All Inputs
$V_{OH}$	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
$V_{OL}$	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
$T_A$	Operating Temperature	0	70	-40	85	°C	

Note b:  $I_{CC1}$  is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: Bringing  $E \geq V_{IH}$  or  $S \leq V_{IL}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note d:  $I_{CC2}$  is the average current required for the duration of the store cycle ( $t_{STORE}$ ) after the sequence ( $t_{WC}$ ) that initiates the cycle.

## AC TEST CONDITIONS

Input Pulse Levels.....	$V_{SS}$ to 3V
Input Rise and Fall Times.....	$\leq 5ns$
Input and Output Timing Reference Levels.....	1.5V
Output Load.....	See Figure 1

CAPACITANCE ( $T_A=25^\circ C$ ,  $f=1.0MHz$ )<sup>e</sup>

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
$C_{IN}$	Input Capacitance	5	pF	$\Delta V = 0$ to 3V
$C_{OUT}$	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note e: These parameters are guaranteed but not tested.

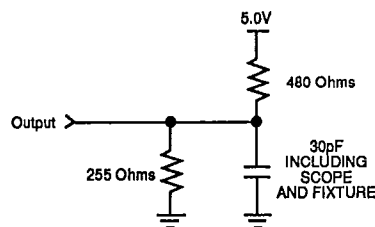


Figure 1: AC Output Loading

## READ CYCLES #1 &amp; #2

 $(V_{CC} = 5.0V \pm 10\%)$ 

NO.	SYMBOLS		PARAMETER	STK14C68-25		STK14C68-30		STK14C68-35		STK14C68-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{ELOV}^1, t_{SHOV}^1$	$t_{ACS}$	Chip Enable Access Time		25		30		35		45	ns
2	$t_{AVAVR}^2$	$t_{RC}$	Read Cycle Time	25		30		35		45		ns
3	$t_{AVOV}^3$	$t_{AA}$	Address Access Time		25		30		35		45	ns
4	$t_{GLOV}^4$	$t_{OE}$	Output Enable to Data Valid		12		15		20		25	ns
5	$t_{AXOX}^5$	$t_{OH}$	Output Hold After Address Change	5		5		5		5		ns
6	$t_{ELOX}^6, t_{SHOX}^6$	$t_{LZ}$	Chip Enable to Output Active	5		5		5		5		ns
7	$t_{EHOZ}^7, t_{SLOZ}^7$	$t_{HZ}$	Chip Disable to Output Inactive		13		15		17		20	ns
8	$t_{GLOX}^8$	$t_{OLZ}$	Output Enable to Output Active	0		0		0		0		ns
9	$t_{GHOZ}^9$	$t_{OHZ}$	Output Disable to Output Inactive		13		15		17		20	ns
10	$t_{ELICCH}^{10}, t_{SHICCH}^{10}$	$t_{PA}$	Chip Enable to Power Active	0		0		0		0		ns
11	$t_{EHICCL}^{11}, t_{SLICCL}^{11}$	$t_{PS}$	Chip Disable to Power Standby		25		25		25		25	ns
11A	$t_{WHOV}^{11A}$	$t_{WR}$	Write Recovery Time		30		35		45		55	ns

Note c: Bringing  $\bar{E}$  high or S low will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

Note e: Parameter guaranteed but not tested.

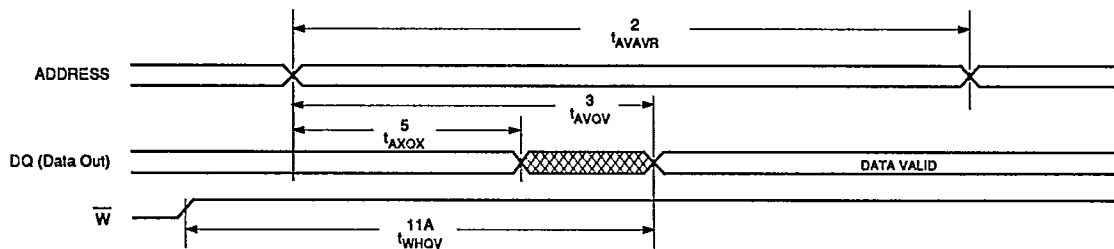
Note f:  $\bar{NE}$  must be high during entire cycle.

Note g: For READ CYCLE #1 and #2,  $\bar{W}$  and  $\bar{NE}$  must be high for entire cycle.

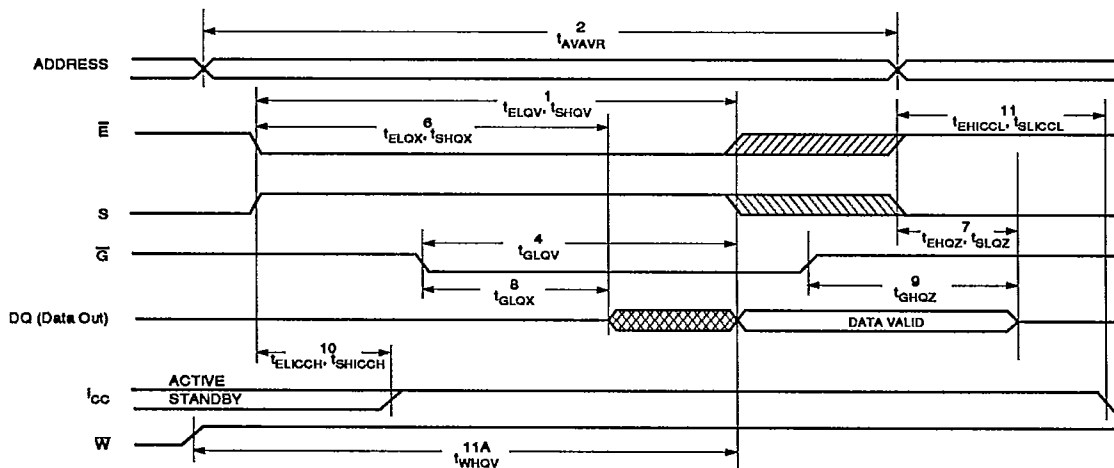
Note h: Device is continuously selected with  $\bar{E}$  low, S high, and  $\bar{G}$  low.

Note i: Measured  $\pm 200mV$  from steady state output voltage.

## READ CYCLE #1 f,g,h



## READ CYCLE #2 f,g



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WRITE CYCLES #1 & #2;  $\bar{G}$  high (this table is effective 3/31/94) $(V_{CC} = 5.0V \pm 10\%)$ 

NO.	SYMBOLS			PARAMETER	STK14C68-25		STK14C68-30		STK14C68-35		STK14C68-45		UNITS
	#1	#2	Ail		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{AVAW}$	$t_{AVAW}, t_{WLSL}$	$t_{WC}$	Write Cycle Time	25		30		35		45		ns
13	$t_{WLWH}$	$t_{WLEH}, t_{WLSL}$	$t_{WP}$	Write Pulse Width	20		25		30		35		ns
14	$t_{ELWH}$	$t_{ELEH}, t_{SHSL}$	$t_{CW}$	Chip Enable to End of Write	20		25		30		35		ns
15	$t_{DVWH}$	$t_{DVEH}, t_{DVSL}$	$t_{DW}$	Data Set-up to End of Write	12		15		18		20		ns
16	$t_{WHDX}$	$t_{EHDX}, t_{SLDX}$	$t_{DH}$	Data Hold After End of Write	0		0		0		0		ns
17	$t_{AVWH}$	$t_{AVEH}, t_{AVSL}$	$t_{AW}$	Address Set-up to End of Write	20		25		30		35		ns
18	$t_{AVWL}$	$t_{AVEL}, t_{AVSH}$	$t_{AS}$	Address Set-up to Start of Write	0		0		0		0		ns
19	$t_{WHAX}$	$t_{EHAX}, t_{SLAX}$	$t_{WR}$	Address Hold After End of Write	0		0		0		0		ns

WRITE CYCLES #1 & #2;  $\bar{G}$  low

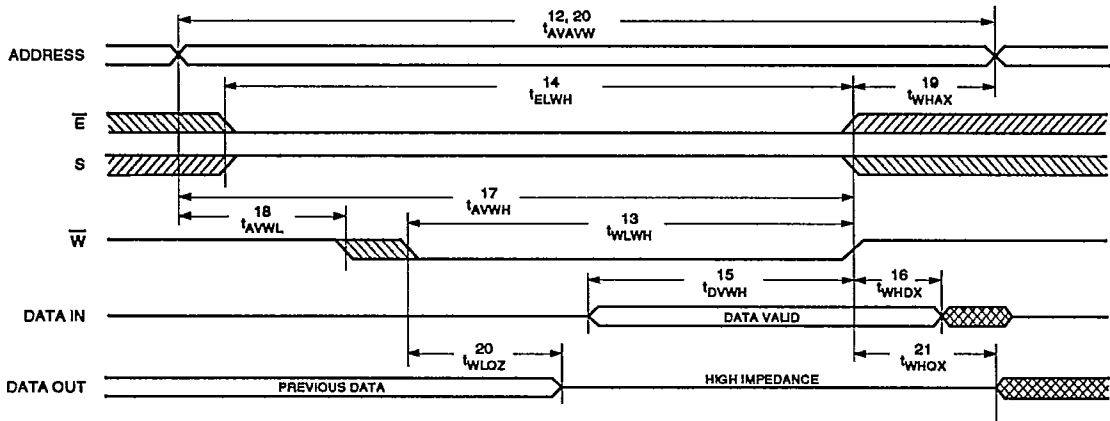
NO.	SYMBOLS			PARAMETER	STK14C68-25		STK14C68-30		STK14C68-35		STK14C68-45		UNITS
	#1	#2	Ail		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{AVAW}$	$t_{AVAW}$	$t_{WC}$	Write Cycle Time	45		45		45		45		ns
13	$t_{WLWH}$	$t_{WLEH}, t_{WLSL}$	$t_{WP}$	Write Pulse Width	35		35		35		35		ns
14	$t_{ELWH}$	$t_{ELEH}, t_{SHSL}$	$t_{CW}$	Chip Enable to End of Write	35		35		35		35		ns
15	$t_{DVWH}$	$t_{DVEH}, t_{DVSL}$	$t_{DW}$	Data Set-up to End of Write	30		30		30		30		ns
16	$t_{WHDX}$	$t_{EHDX}, t_{SLDX}$	$t_{DH}$	Data Hold After End of Write	0		0		0		0		ns
17	$t_{AVWH}$	$t_{AVEH}, t_{AVSL}$	$t_{AW}$	Address Set-up to End of Write	35		35		35		35		ns
18	$t_{AVWL}$	$t_{AVEL}, t_{AVSH}$	$t_{AS}$	Address Set-up to Start of Write	0		0		0		0		ns
19	$t_{WHAX}$	$t_{EHAX}, t_{SLAX}$	$t_{WR}$	Address Hold After End of Write	0		0		0		0		ns
20	$t_{WLOZ}^{1m}$		$t_{WZ}$	Write Enable to Output Disable		35		35		35		35	ns
21	$t_{WHQX}$		$t_{OW}$	Output Active After End of Write	5		5		5		5		ns

Note f:  $\bar{NE}$  must be  $\geq V_{IH}$  during entire cycle.

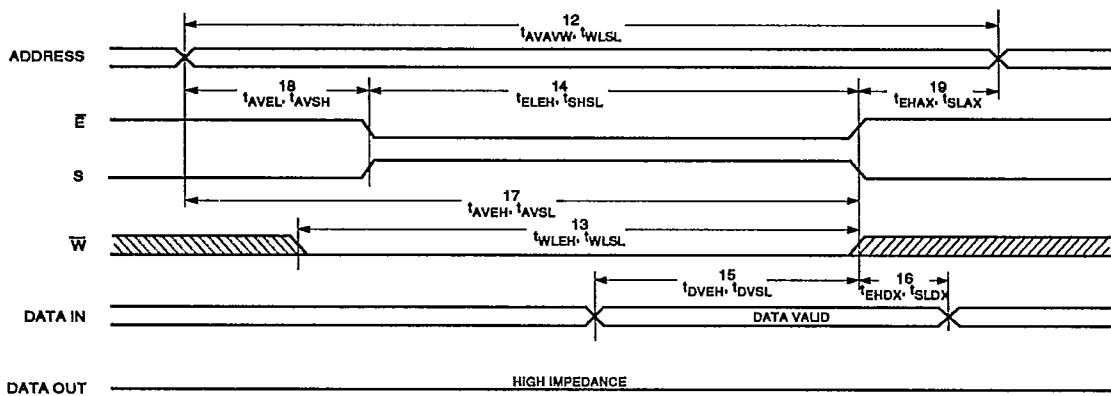
Note i: Measured  $\pm 200mV$  from steady state output voltage.

Note K:  $\bar{E}$  or  $\bar{W}$  must be  $\geq V_{IH}$  during address transitions.

Note m: If  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1:  $\bar{W}$  CONTROLLED<sup>f,k</sup>

2

WRITE CYCLE #2:  $\bar{E}$  CONTROLLED<sup>f,k</sup>

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# NONVOLATILE MEMORY OPERATION

## MODE SELECTION

S	$\bar{E}$	$\bar{W}$	$\bar{G}$	$\bar{NE}$	MODE	POWER
L	X	X	X	X	Not Selected	Standby
H	H	X	X	X	Not Selected	Standby
H	L	H	L	H	Read RAM	Active
H	L	L	X	H	Write RAM	Active
H	L	H	L	L	Nonvolatile <i>RECALL</i> <sup>n</sup>	Active
H	L	L	H	L	Nonvolatile <i>STORE</i>	$I_{CC2}$
H	L	L	L	L	No operation	Active
H	L	H	H	X		

## STORE CYCLES #1 & #2

 $(V_{CC} = 5.0V \pm 10\%)$ 

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	AIL				
22	$t_{WLOX}^p$	$t_{ELOXS} \cdot t_{SHOXS}$	$t_{STORE}$	STORE Cycle Time		10	ms
23	$t_{WLNH}^q$	$t_{ELNHS} \cdot t_{SHNHS}$	$t_{WC}$	STORE Initiation Cycle Time	25		ns
24	$t_{GHNL}$			Output Disable Set-up to $\bar{NE}$ Fall	5		ns
25		$t_{GHLEL} \cdot t_{GHSH}$		Output Disable Set-up to $\bar{E}$ Fall	5		ns
26	$t_{NLWL}$	$t_{NLEL} \cdot t_{NLSH}$		$\bar{NE}$ Set-up	5		ns
27	$t_{ELWL} \cdot t_{SHWL}$			Chip Enable Set-up	5		ns
28		$t_{WLEL} \cdot t_{WLSH}$		Write Enable Set-up	5		ns

Note n: An automatic *RECALL* also takes place at power up, starting when  $V_{CC}$  exceeds 4.1V, and taking  $t_{RECALL}$  from the time at which  $V_{CC}$  exceeds 4.5V.

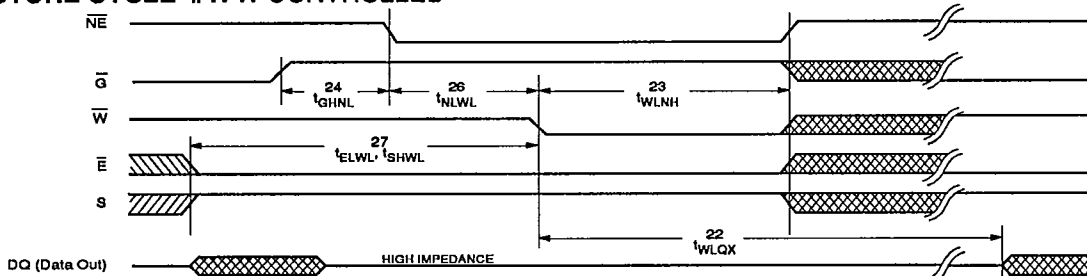
$V_{CC}$  must not drop below 4.1V once it has exceeded it for the *RECALL* to function properly.

Note o: If  $\bar{E}$  is low and S is high for any period of time in which  $\bar{W}$  is high while  $\bar{G}$  and  $\bar{NE}$  are low, then a *RECALL* cycle may be initiated.

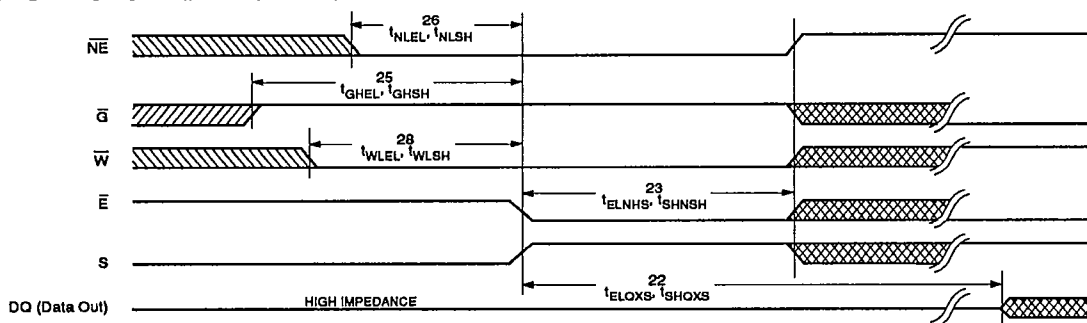
Note p: Measured with  $\bar{W}$  and  $\bar{NE}$  both returned high, and  $\bar{G}$  returned low. Note that *STORE* cycles are inhibited/aborted by  $V_{CC} < 4.1V$  (*STORE* Inhibit).

Note q: Once  $t_{WC}$  has been satisfied by  $\bar{NE}$ ,  $\bar{G}$ ,  $\bar{W}$ , S and  $\bar{E}$ , the *STORE* cycle is completed automatically. Any of  $\bar{NE}$ ,  $\bar{G}$ ,  $\bar{W}$ , S or  $\bar{E}$  may be used to terminate the *STORE* initiation cycle.

## STORE CYCLE #1: $\bar{W}$ CONTROLLED<sup>o</sup>



## STORE CYCLE #2: $\bar{E}$ or S CONTROLLED<sup>o</sup>



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## RECALL CYCLES #1, #2 &amp; #3

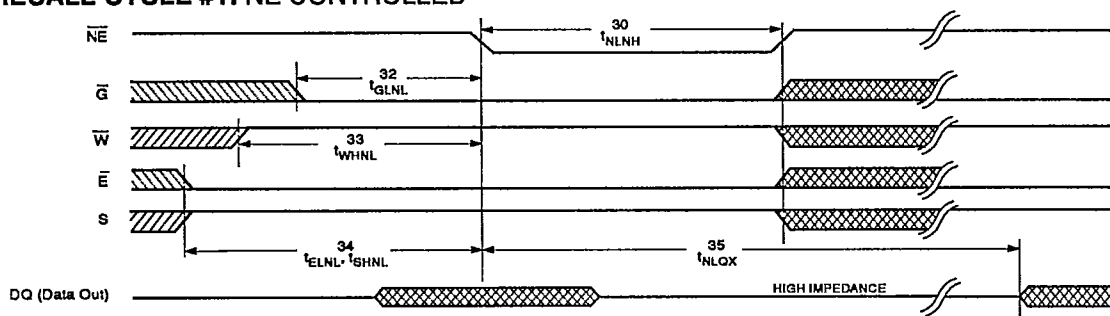
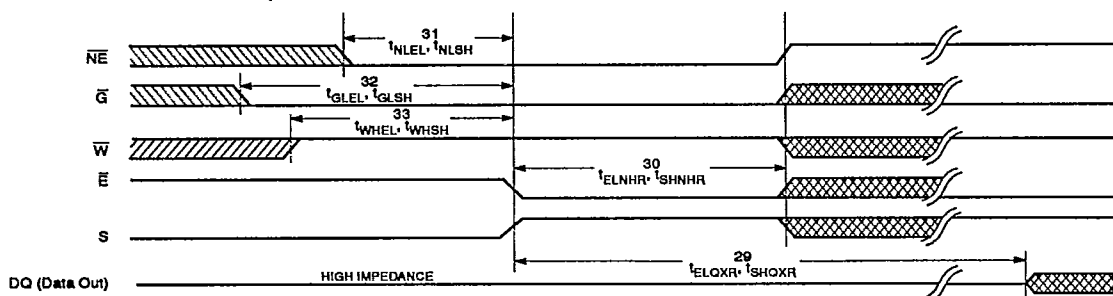
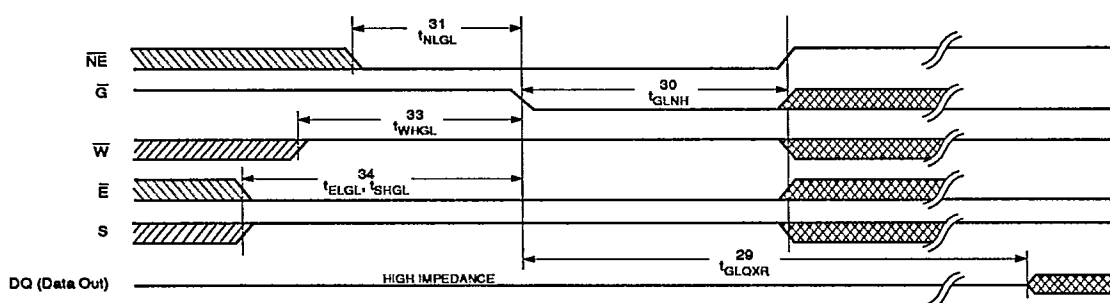
 $(V_{CC} = 5.0V \pm 10\%)$ 

NO.	SYMBOLS			PARAMETER	MIN	MAX	UNTS
	#1	#2	#3				
29	$t_{NLOX}^{\dagger}$	$t_{ELOXR}^{\dagger}$ $t_{SHOXR}^{\dagger}$	$t_{GLOXR}^{\dagger}$	RECALL Cycle Time		20	$\mu s$
30	$t_{NLNH}^{\dagger}$	$t_{ELNHR}^{\dagger}$ $t_{SHNHR}^{\dagger}$	$t_{GLNH}^{\dagger}$	RECALL Initiation Cycle Time	25		ns
31		$t_{NLEL}^{\dagger}$ $t_{NLSH}^{\dagger}$	$t_{NLGL}^{\dagger}$	$\overline{NE}$ Set-up	0		ns
32	$t_{GLNL}^{\dagger}$	$t_{GLEL}^{\dagger}$ $t_{GLSH}^{\dagger}$		Output Enable Set-up	0		ns
33	$t_{WHNL}^{\dagger}$	$t_{WHEL}^{\dagger}$ $t_{WHSH}^{\dagger}$	$t_{WHGL}^{\dagger}$	Write Enable Set-up	0		ns
34	$t_{ELNL}^{\dagger}$ $t_{SHNL}^{\dagger}$		$t_{ELGL}^{\dagger}$ $t_{SHGL}^{\dagger}$	Chip Enable Set-up	0		ns
35	$t_{NLOZ}^{\dagger}$					25	ns

Note r: Measured with S,  $\overline{W}$  and  $\overline{NE}$  high, and  $\overline{G}$  and  $\overline{E}$  low.

Note s: Once  $t_{NLNH}$  has been satisfied by  $\overline{NE}$ ,  $\overline{G}$ ,  $\overline{W}$ , S and  $\overline{E}$ , the RECALL cycle is completed automatically. Any of  $\overline{NE}$ ,  $\overline{G}$ , S or  $\overline{E}$  may be used to terminate the RECALL initiation cycle.

Note t: If  $\overline{W}$  is low at any point in which both  $\overline{E}$  and  $\overline{NE}$  are low and  $\overline{G}$  and S are high, then a STORE cycle will be initiated instead of a RECALL.

RECALL CYCLE #1:  $\overline{NE}$  CONTROLLED<sup>o</sup>RECALL CYCLE #2:  $\overline{E}$ , S CONTROLLED<sup>o</sup>RECALL CYCLE #3:  $\overline{G}$  CONTROLLED<sup>o,t</sup>

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## DEVICE OPERATION

The STK14C68 has two modes of operation: SRAM mode and nonvolatile mode, determined by the state of the  $\overline{NE}$  pin. When in SRAM mode, the memory operates as an ordinary static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

### SRAM READ

The STK14C68 performs a READ cycle whenever  $\overline{E}$  and  $\overline{G}$  are LOW and S,  $\overline{NE}$  and  $\overline{W}$  are HIGH. The address specified on pins  $A_{0-12}$  determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (READ CYCLE #1). If the READ is initiated by S,  $\overline{E}$  or  $\overline{G}$ , the outputs will be valid at  $t_{SHOV}$ ,  $t_{ELQV}$  or  $t_{GLQV}$  whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{E}$  or  $\overline{G}$  is brought HIGH or S,  $\overline{W}$  or  $\overline{NE}$  is brought LOW.

### SRAM WRITE

A write cycle is performed whenever  $\overline{E}$  and  $\overline{W}$  are LOW and  $\overline{NE}$  and S are HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{E}$  or  $\overline{W}$  go HIGH or S goes LOW at the end of the cycle. The data on pins  $DQ_{0-7}$  will be written into the memory if it is valid  $t_{DVWH}$  before the end of a  $\overline{W}$  controlled WRITE or  $t_{DVEH}$  ( $t_{DVSL}$ ) before the end of an  $\overline{E}$  (S) controlled WRITE.

It is recommended that  $\overline{G}$  be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If  $\overline{G}$  is left LOW, internal circuitry will turn off the output buffers  $t_{WLOZ}$  after  $\overline{W}$  goes LOW.

### NONVOLATILE STORE

A STORE cycle is performed when  $\overline{NE}$ ,  $\overline{E}$  and  $\overline{W}$  are LOW and  $\overline{G}$  and S are HIGH. While any sequence to achieve this state will initiate a STORE, only  $\overline{W}$  initiation (STORE CYCLE #1) and  $\overline{E}$  (or S) initiation (STORE CYCLE #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a STORE cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a STORE cycle is initiated, further

input and output are disabled and the  $DQ_{0-7}$  pins are tri-stated until the cycle is completed.

If  $\overline{E}$  and  $\overline{G}$  are LOW and S,  $\overline{W}$  and  $\overline{NE}$  are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the STORE.

### HARDWARE PROTECT

The STK14C68 offers two levels of protection to suppress inadvertent STORE cycles. If the control signals ( $\overline{E}$ , S,  $\overline{G}$ ,  $\overline{W}$ , and  $\overline{NE}$ ) remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will not be started. The STORE (or RECALL) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the STK14C68 offers hardware protection through  $V_{CC}$  Sense. A STORE cycle will not be initiated, and one in progress will discontinue if  $V_{CC}$  goes below 4.1V. 4.1V is a typical, characterized value.

### NONVOLATILE RECALL

A RECALL cycle is performed when  $\overline{E}$ ,  $\overline{G}$ , and  $\overline{NE}$  are LOW and S and  $\overline{W}$  are HIGH. Like the STORE cycle, RECALL is initiated when the last of the five clock signals goes to the RECALL state. Once initiated, the RECALL cycle will take  $t_{NLOX}$  to complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pins will take effect.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the STORE cycle, a transition must occur on some control pin to cause a recall, preventing inadvertent multi-triggering. On power-up, once  $V_{CC}$  exceeds the  $V_{CC}$  Sense voltage of 4.1V, a RECALL cycle is automatically initiated. The voltage on the  $V_{CC}$  pin must not drop below 4.1V once it has risen above it in order for the RECALL to operate properly. Due to this automatic RECALL, SRAM operation cannot commence until  $t_{NLOX}$  after  $V_{CC}$  exceeds 4.1V. 4.1V is a typical, characterized value.



## ORDERING INFORMATION

**2****STK14C68 - 5 C 30 I****Temperature Range**

blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

**Access Time**

25 = 25ns

30 = 30ns

35 = 35ns

45 = 45ns

**Package**

P = Plastic 28 pin 300 mil DIP

S = Plastic 28 pin SOIC

C = Ceramic 28 pin 300 mil DIP

**Retention / Endurance**

blank = 10 years / 10,000 cycles

5 = 10 years / 100,000 cycles