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FPGA to ASIC Conversion

Partnership Program for legacy program support

Issue:	Date:	Approval:	Dept:
1	10/03/10	MS	Eng

Overview

- **Force with its design partnership have been migrating FPGA designs to ASICs for over a decade**
  - Cost reduction for existing FPGA production volumes
  - Providing a pin for pin FPGA migration to ASIC
  - Integration of multiple FPGAs into one ASIC
  - Extending production support for End of Life FPGAs

- **Optional conversion approaches supported:**
  - RTL handoff
  - FPGA Netlist handoff

Benefits of Conversion to Structured ASIC

- Pin for pin device conversion-no board re-layout
  - When technically feasible
- Increased performance or performance margin
- Significant reduction in power consumption
  - Ideal for green initiative
- Overall Reduction in device BOM cost
  - Up to 80% cost reduction
- Freeing up more real estate
  - Integration of multiple FPGAs into one
  - Smaller Structured ASIC devices and packages
  - Elimination of PROM/EPROM programming part

Conversion Objectives

- **Ensure first time success by reducing risk**
  - Work methodically using proven flows
  - Use reputable industry standard tools
  - Verify work done and results throughout the process
  - Confirm performance against expectations
- **Minimise customer involvement**
  - Leverage available deliverables
  - Involve customer only when absolutely necessary

Project Assessment and Requirements Review

- **Most important phase of the project**
- **Gain understanding of:**
  - Available deliverables
  - Overall design requirements
- **Assess project risks**
- **Communicate migration process to customer including risk mitigation plan**
- **Communicate project feasibility, schedule and expectations**

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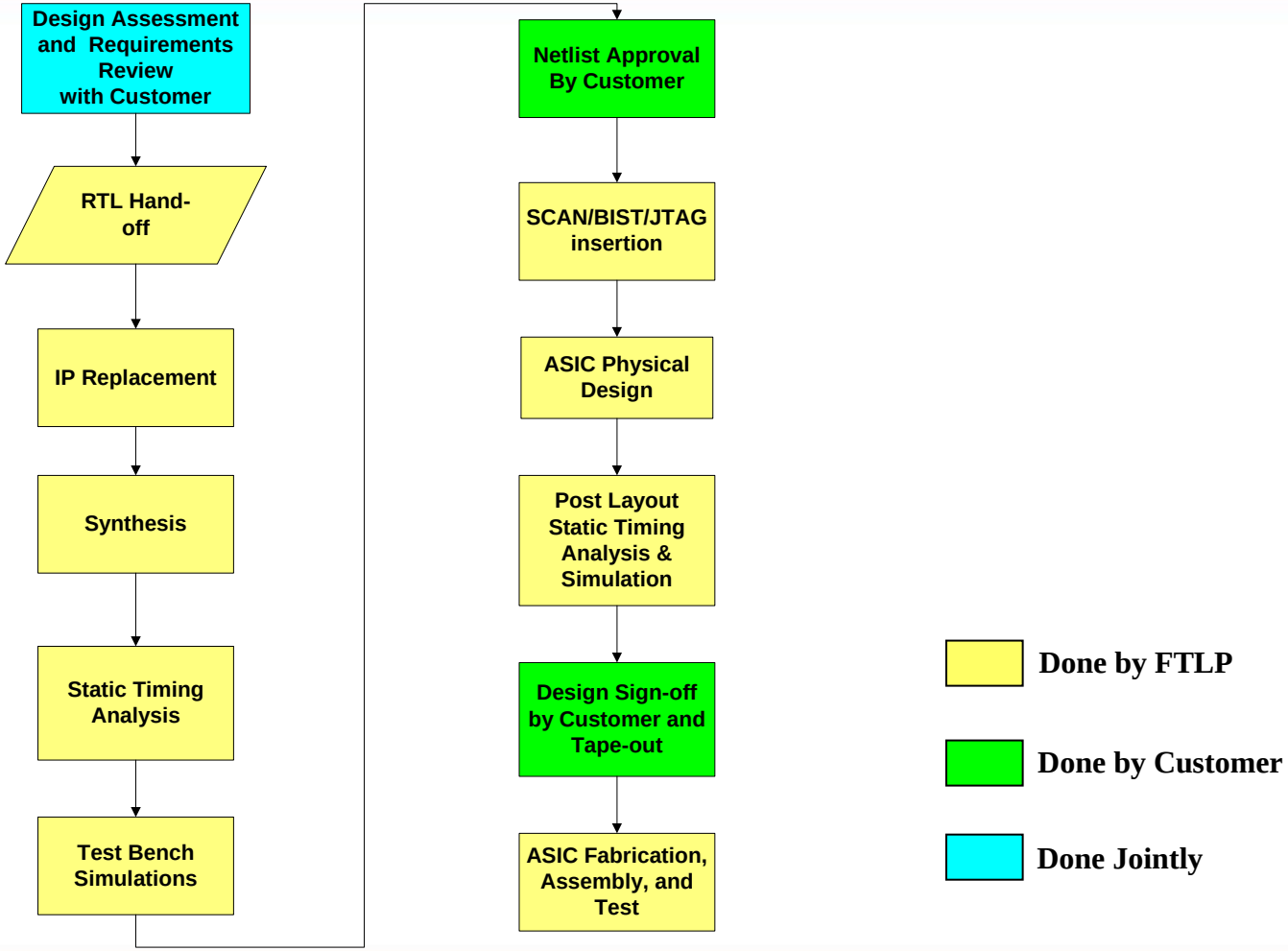
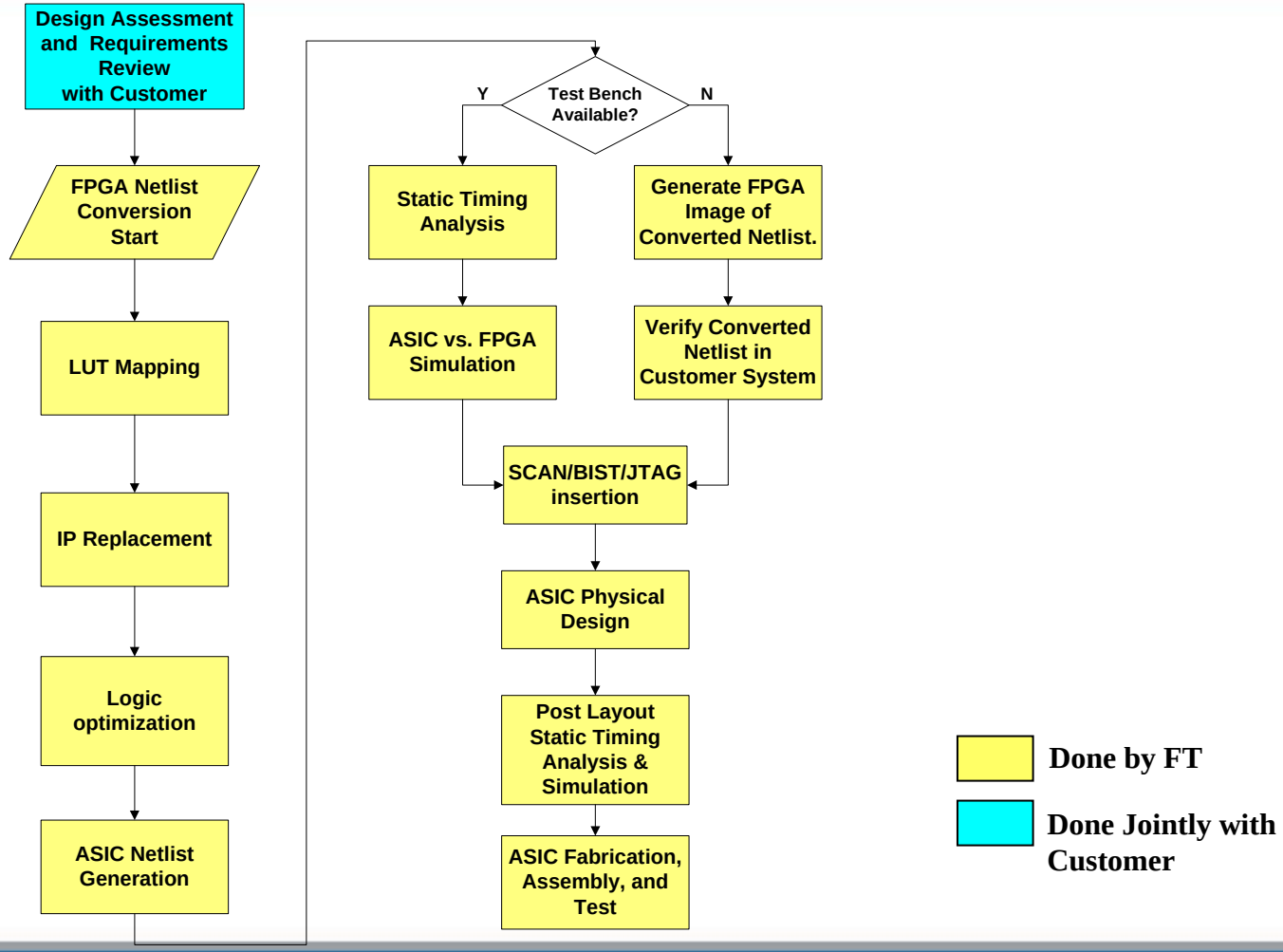
Customer Deliverables

- RTL code or FPGA Netlist → Either one is acceptable
- 3rd party IP specifications (if applicable) → Feasibility depends on:
  - Information available
  - Possibility of replacement
- Constraints
  - Internal
  - External (I/O)
  → Very important to insure design meets timing
- Test bench and/or test vectors (If available) → If not available, generate FPGA image and verify or leverage 3rd party consultant
- Pin-out and packaging information → Usually available with system design information

Conversion Flow With RTL Hand-off



Conversion Flow with FPGA Netlist Handoff



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Industry Standard Tools

- **Front-end**
  - **Simulation**
    - **NC-Verilog, Verilog-XL, VHDL**
  - **RTL Analysis and Synthesis**
    - **Synopsys: DC Shell, DC Ultra**
    - **Magma: Blast Create**
  - **Formal Verification**
    - **Synopsys Formality**
- **Back End**
  - **DFT Insertion and ATPG**
    - Syntest
  - **Placement**
    - Magma Blast Fusion
  - **Clock Tree Generation**
    - Magma Blast Fusion
  - **Extraction**
    - Magma Blast Fusion
  - **Place and Route (new)**
    - Magma: Blast Fusion

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FPGA Conversion Summary

- **FTL Specialised in migrating FPGAs to ASICs**
- **FTL Utility identifies appropriate FTL masterslice that maps to FPGA from one of the following companies:**
  - Actel, Altera, Atmel, Cypress, Lattice, QuickLogic, Xilinx
- **FTL will assess the project and provide details on:**
  - Recommended FTL process technology to target
  - Associated cost savings
  - Estimated power reduction, etc.
  - Required efforts
  - Schedule to implement conversion
  - Any potential areas of risk and contingencies