

64K -bit/32K -bit 2-WIRE SERIAL CMOS EEPROM

FEATURES

- Low Power CMOS Technology
 - Standby Current less than 10 μ A (5.5V)
 - Read Current (typical) less than 1 mA (5.5V)
 - Write Current (typical) less than 3 mA (5.5V)
- Low Voltage Operation
 - FT24C64-2 & FT24C32-2: Vcc = 1.8V to 5.5V
 - FT24C64-3 & FT24C32-3: Vcc = 2.5V to 5.5V
- 100 KHz (1.8V) and 400 KHz (5V) Compatibility
- Hardware Data Protection
 - Write Protect Pin
- Sequential Read Feature
- Filtered Inputs for Noise Suppression
- 8-pin SBDIP
- Self time write cycle with auto clear
 - 5 ms @ 2.5V
- Organization:
 - FT24C64-2 and FT24C64-3: 8192x8
 - FT24C32-2 and FT24C32-3: 4096x8
- 32-Byte Page Write Buffer
- Two-Wire Serial Interface
 - Bi-directional data transfer protocol
- High Reliability
 - Endurance: 1,000,000 Cycles
 - Data Retention: 100 Years
- Commercial and Industrial temperature ranges

PRODUCT OFFERING OVERVIEW

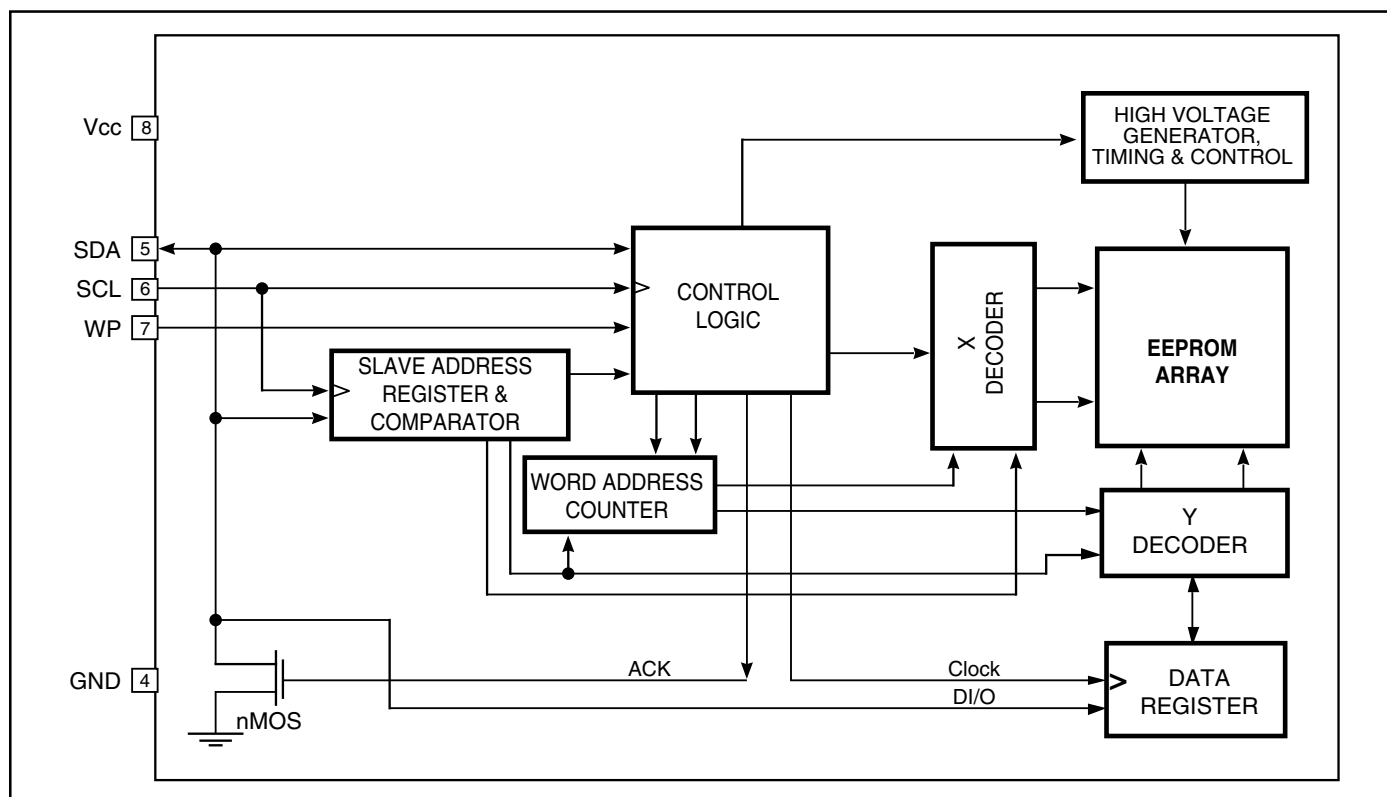
Part No	Voltage	Speed	Standby ICC	Read ICC	Write ICC	Temperature
FT24C64-2	1.8V-5.5V	100 KHz	< 5 μ A	1 mA	3 mA	C,I,M
FT24C64-3	2.5V-5.5V	400 KHz	< 10 μ A	1 mA	3 mA	C,I,M
FT24C32-2	1.8V-5.5V	100 KHz	< 5 μ A	1 mA	3 mA	C,I,M
FT24C32-3	2.5V-5.5V	400 KHz	< 10 μ A	1 mA	3 mA	C,I,M

1. DESCRIPTION

The FT24C64-2 is a 1.8V (1.8V-5.5V) 64K-bit (8192 x 8) Electrically Erasable PROM, FT24C64-3 is a 2.5V (2.5V-5.5V) 64K-bit (8192 x 8) Electrically Erasable PROM, FT24C32-2 is a 1.8V (1.8V-5.5V) 32K-bit (4096 x 8) Electrically Erasable PROM and the FT24C32-3 is a 2.5V (2.5V-5.5V) 32K-bit (4096 x 8) Electrically Erasable PROM.

The FT24CXX (FT24C64-2, FT24C64-3, FT24C32-2 and FT24C32-3) family is a low-cost and low voltage 2-wire Serial EEPROM. It is fabricated using advanced CMOS EEPROM technology and provides a low power and low voltage operation. The FT24CXX family features a write protection feature, and is available in 8-pin SBDIP package.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

A0-A2	Address Inputs
SDA	Serial Address/Data I/O
SCL	Serial Clock Input
WP	Write Protect Input
Vcc	Power Supply
GND	Ground

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

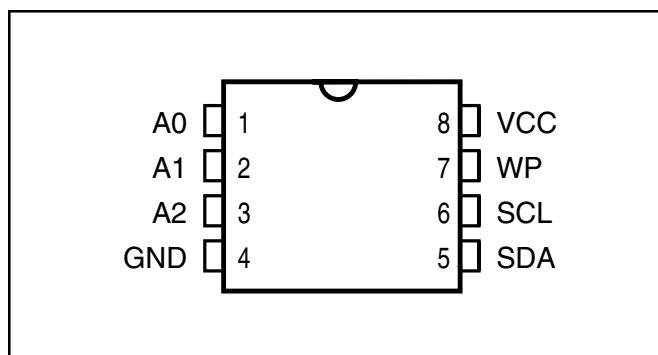
SDA

The SDA is a Bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wire-Or'd with other open drain or open collector outputs. The SDA bus *requires* a pullup resistor to Vcc.

A0, A1, A2

The A0, A1 and A2 are the device address inputs that are hardwired or left not connected for hardware compatibility

8-LEAD SBDIP



with the FT24C16. When pins are hard-wired, as many as eight 32K/64K devices may be addressed on a single bus system. When the pins are not hard-wired, the default A0, A1, and A2 are zero..

WP

WP is the Write Protect pin. If the WP pin is tied to Vcc the entire array becomes Write Protected (Read only). When WP is tied to GND or left floating normal read/write operations are allowed to the device.

4. DEVICE OPERATION

The FT24CXX family features a serial communication and supports a bi-directional 2-wire bus transmission protocol.

4.1 2-WIRE BUS

The two-wire bus is defined as a Serial Data line (SDA), and a Serial Clock Line (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as a receiver. The bus is controlled by MASTER device which generates the SCL, controls the bus access and generates the STOP and START conditions. The FT24CXX is the SLAVE device on the bus.

4.2 The Bus Protocol:

- Data transfer may be initiated only when the bus is not busy
- During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

The state of the data line represents valid data when after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the SDA line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.

4.3 START Condition

The START condition precedes all commands to the device and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The FT24CXX monitors the SDA and SCL lines and will not respond until the START condition is met.

4.4 STOP Condition

The STOP condition is defined as a LOW to HIGH transition of SDA when SCL is HIGH. All operations must end with a STOP condition.

4.5 Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line.

5. DEVICE ADDRESSING

The MASTER begins a transmission by sending a START condition. The MASTER then sends the address of the particular slave device it is requesting. The SLAVE (Fig. 5) address is 8 bits. The four most significant bits of the address are fixed as 1010 for the FT24CXX. The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus.

These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the MASTER sends a START condition and the SLAVE address byte, the FT24CXX monitors the bus and responds with an Acknowledge (on the SDA line) when its address matches the transmitted slave address. The FT24CXX pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data. The FT24CXX then performs a Read or Write operation depending on the state of the R/W bit.

6. WRITE OPERATION

6.1 Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two byte addresses that are to be written into the address pointer of the FT24CXX. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the address memory location. The IS24CXX acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

6.2 Page Write

The FT24CXX is capable of 32-byte page-WRITE operation. A page-WRITE is initiated in the same manner as a byte write, but instead of terminating the internal write cycle after the first data word is transferred, the master device can transmit up to 31 more bytes. After the receipt of each data word, the FT24CXX responds immediately with an ACKnowledge on SDA line, and the five lower order data word address bits are internally incremented by one, while the five higher order bits of the data word address remain constant. If the master device should transmit more than 32 words, prior to issuing the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. Once all 32 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the FT24CXX in a single write cycle. All inputs are disabled until completion of the internal WRITE cycle.

6.3 Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the FT24CXX initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the FT24CXX is still busy with the write operation, no ACK will be returned. If the FT24CXX has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

7. READ OPERATION

READ operations are initiated in the same manner as WRITE operations, except that the read/write bit of the slave address is set to "1". There are three READ operation options: current address read, random address read and sequential read.

7.1 Current Address Read

The FT24CXX contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a read or write operation addressed to the address location n , the internal address counter would increment to address location $n+1$. When the FT24CXX receives the Device Addressing Byte with a READ operation (read/write bit set to "1"), it will respond an Acknowledge and transmit the 8-bit data word stored at address location $n+1$. The master will not acknowledge the transfer but does generate a STOP condition and the FT24CXX discontinues transmission. If ' n ' is the last byte of the memory, then the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

7.2 Random Address Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and word address of the location it wishes to read. After the FT24CXX acknowledges the word address, the Master device resends the START condition and the slave address, this time with the $R/\overline{W}$ bit set to one. The FT24CXX then responds with its acknowledge and sends the data requested. The master device does not send an acknowledge but will generate a STOP condition. (Refer to Figure 9. Random Address Read Diagram.)

7.3 Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the FT24CXX sends initial byte sequence, the master device now responds with an Acknowledge indicating it requires additional data from the FT24CXX. The FT24CXX continues to output data for each Acknowledge received. The master device terminates the sequential READ operation by pulling SDA HIGH (no Acknowledge) indicating the last data word to be read, followed by a STOP condition.

The data output is sequential, with the data from address n followed by the data from address $n+1$, ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential read operation. When the memory address boundary (8191 for FT24C64-2 and FT24C64-3; 4095 for FT24C32-2 and FT24C32-3) is reached, the address counter "rolls over" to address 0, and the FT24CXX-2 continues to output data for each Acknowledge received. (Refer to Figure 10. Sequential Read Operation Starting with a Random Address READ Diagram.)

Figure 1. Typical System Bus Configuration

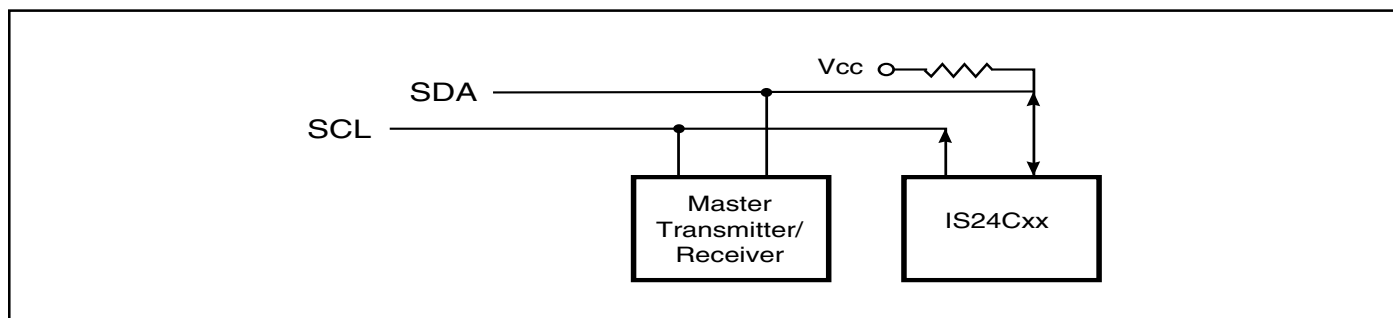


Figure 2. Output Acknowledge

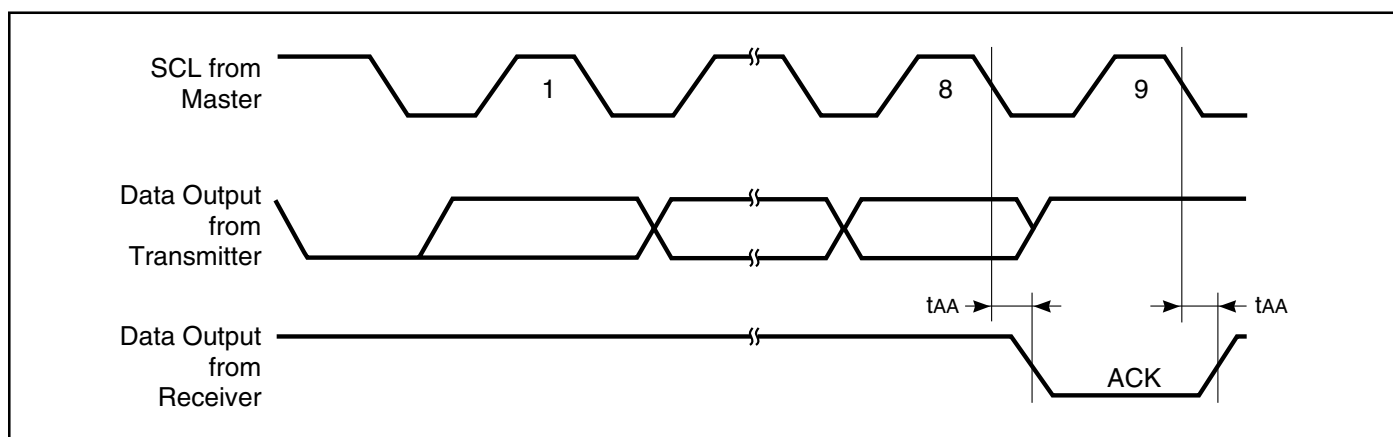


Figure 3. START and STOP Conditions

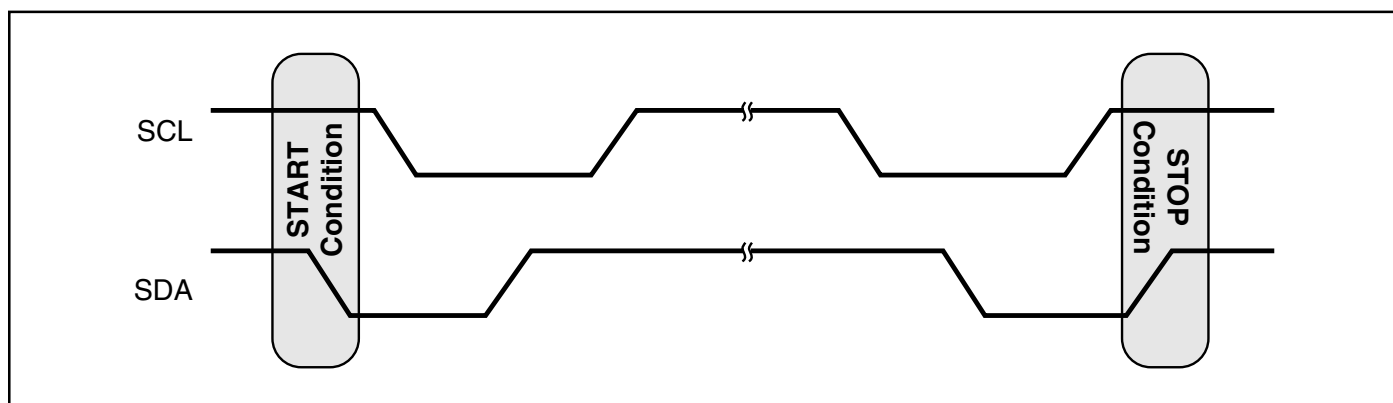


Figure 4. Data Validity Protocol

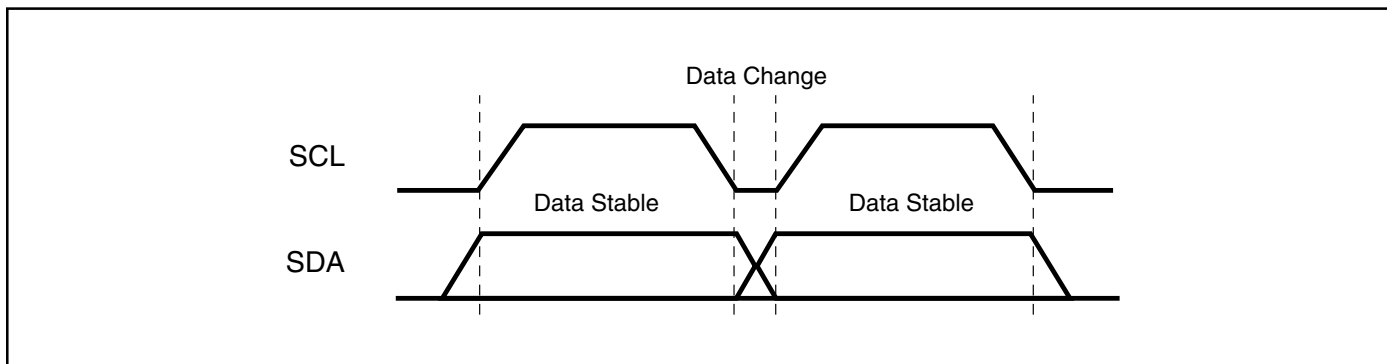


Figure 5. Slave Address

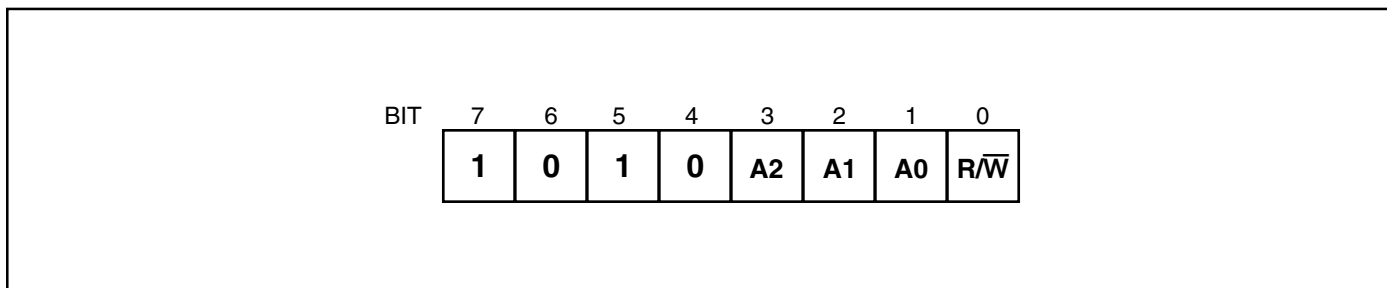


Figure 6. Byte Write

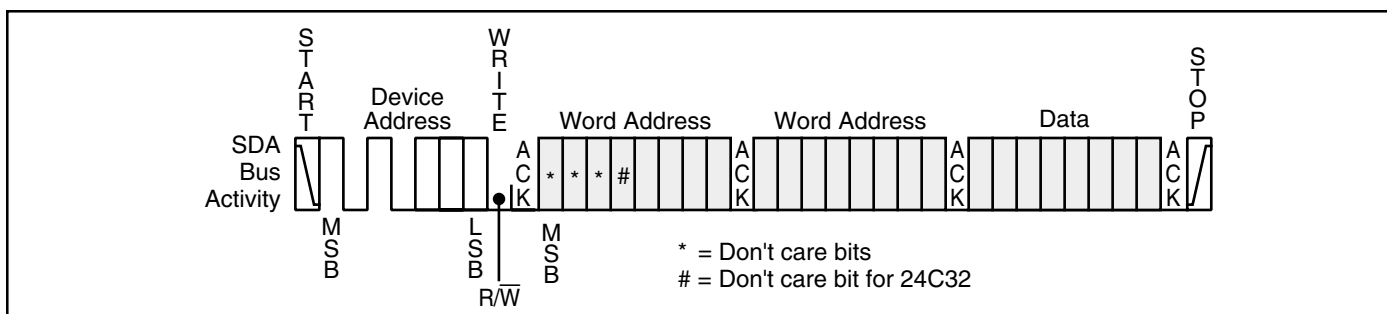


Figure 7. Page Write

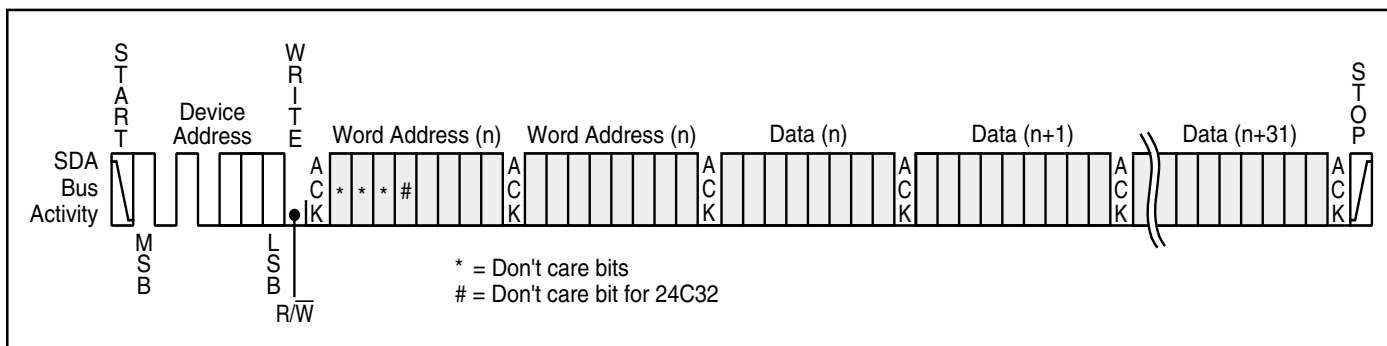


Figure 8. Current Address Read

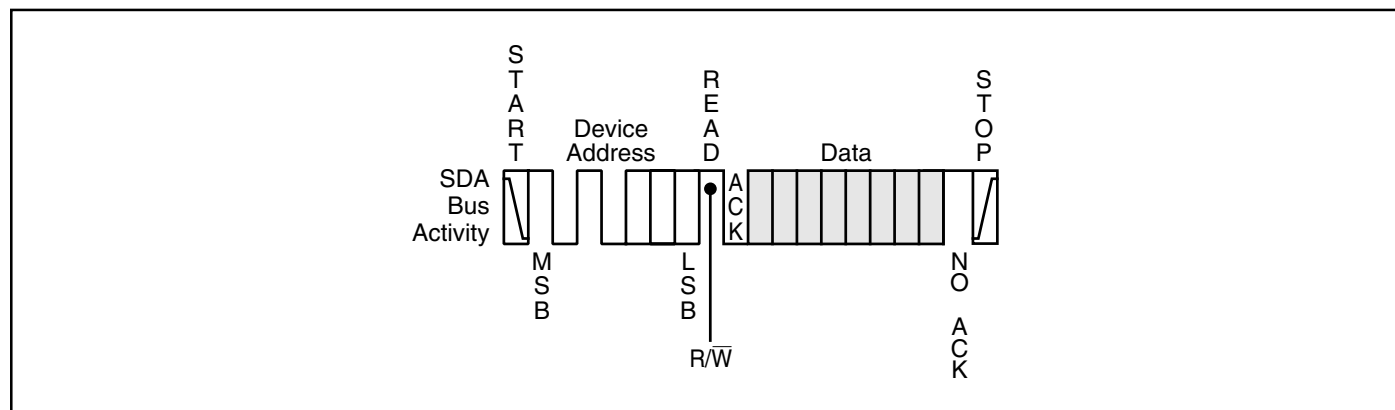


Figure 9. Random Address Read

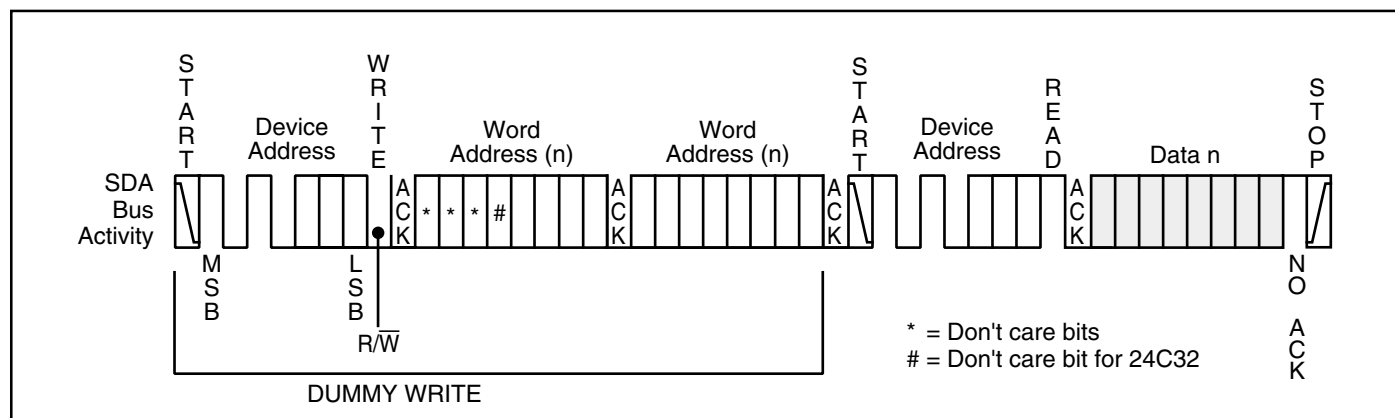
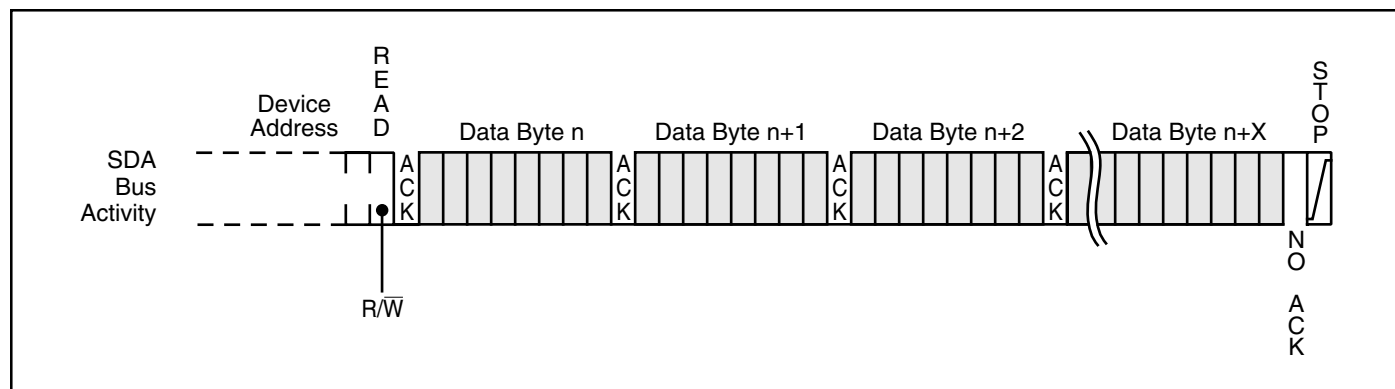


Figure 10. Sequential Read



8. ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _S	Supply Voltage	0.5 to +6.25	V
V _P	Voltage on Any Pin	−0.5 to V _{CC} + 0.5	V
T _{BIAS}	Temperature Under Bias	−40 to +85	°C
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	Output Current	5	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9. OPERATING RANGE (FT24C64-2 and FT24C32-2)

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	1.8V to 5.5V
Industrial	−40°C to +85°C	1.8V to 5.5V

10. OPERATING RANGE (FT24C64-3 and FT24C32-3)

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	2.5V to 5.5V
Industrial	−40°C to +85°C	2.5V to 5.5V

11. CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

12. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OL1}	Output LOW Voltage	V _{CC} = 1.8V, I _{OL} = 0.15 mA	—	0.2	V
V _{OL2}	Output LOW Voltage	V _{CC} = 2.5V, I _{OL} = 1.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		V _{CC} x 0.7	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage		-1.0	V _{CC} x 0.3	V
I _{LI}	Input Leakage Current	V _{IN} = V _{CC} max.	—	3	μA
I _{LO}	Output Leakage Current		—	3	μA

Notes: V_{IL} min and V_{IH} max are reference only and are not tested.

13. POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _{CC1}	V _{CC} Operating Current	READ at 100 KHz (V _{CC} = 5V)	—	1.0	mA
I _{CC2}	V _{CC} Operating Current	WRITE at 100 KHz (V _{CC} = 5V)	—	3.0	mA
I _{SB1}	Standby Current	V _{CC} = 1.8V	—	5	μA
I _{SB2}	Standby Current	V _{CC} = 5.5V	—	10	μA

14. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	1.8V-5.5V		2.5V-5.5V		Unit
			Min.	Max.	Min.	Max.	
f _{SCL}	SCL Clock Frequency		0	100	0	400	KHz
T	Noise Suppression Time ⁽¹⁾		—	100	—	50	ns
t _{LOW}	Clock LOW Period		4.7	—	1.2	—	μs
t _{HIGH}	Clock HIGH Period		4	—	0.6	—	μs
t _{BUF}	Bus Free Time Before New Transmission ⁽¹⁾		4.7	—	1.2	—	μs
t _{SU:STA}	Start Condition Setup Time		4.7	—	0.6	—	μs
t _{SU:STO}	Stop Condition Setup Time		4.7	—	0.6	—	μs
t _{HD:STA}	Start Condition Hold Time		4	—	0.6	—	μs
t _{HD:STO}	Stop Condition Hold Time		4	—	0.6	—	μs
t _{SU:DAT}	Data In Setup Time		200	—	100	—	ns
t _{HD:DAT}	Data In Hold Time		0	—	0	—	ns
t _{DH}	Data Out Hold Time	SCL LOW to SDA Data Out Change	100	—	50	—	ns
t _{AA}	Clock to Output	SCL LOW to SDA Data Out Valid	0.1	4.5	0.1	0.9	μs
t _R	SCL and SDA Rise Time ⁽¹⁾		—	1000	—	300	ns
t _F	SCL and SDA Fall Time ⁽¹⁾		—	300	—	300	ns
t _{WR}	Write Cycle Time		—	10	—	5	ms

Note:

1. This parameter is characterized but not 100% tested.

15. AC WAVEFORMS

Figure 11. Bus Timing

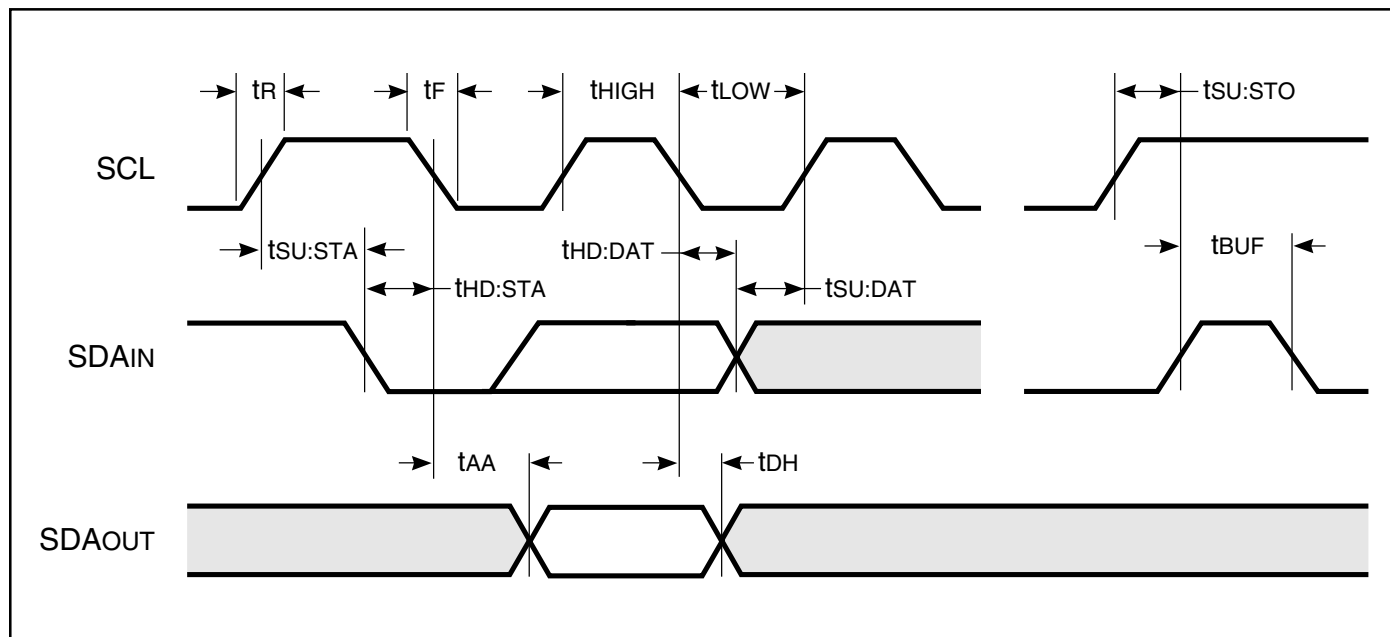
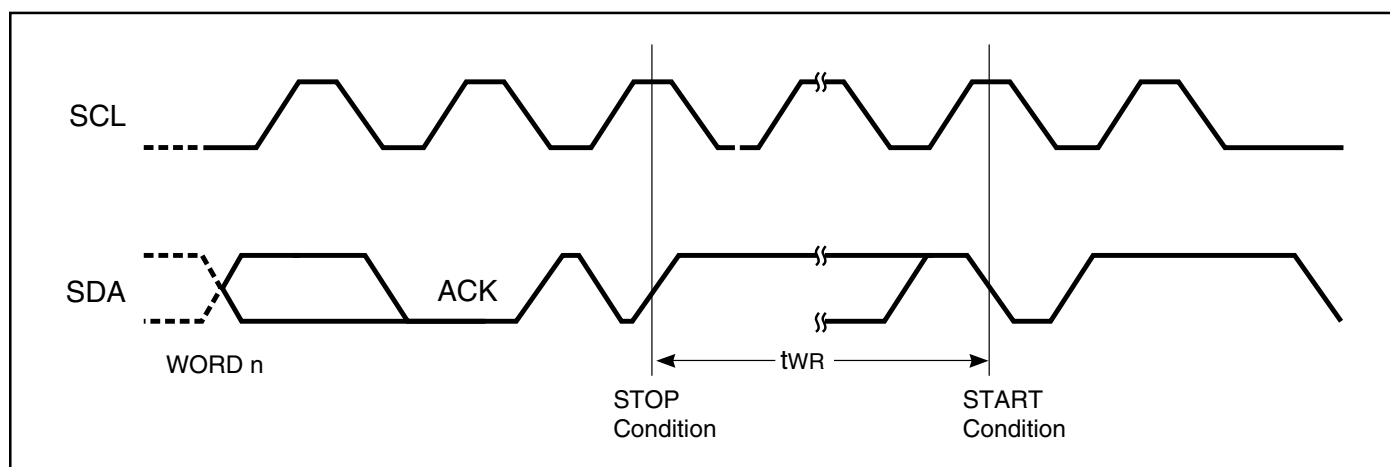


Figure 12. Write Cycle Timing



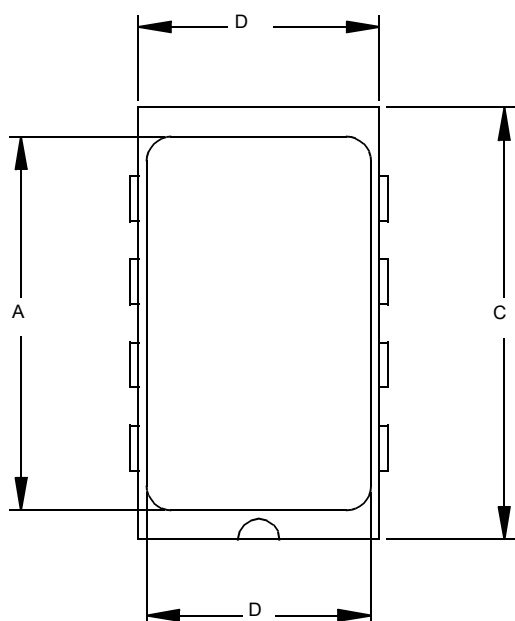
16. Ordering Information

Device Identification	Frequency/ Voltage	Package	Temp/Screening
			C Commercial (0°C to +70°C) I Industrial (-40°C to +85°C) M Military (-55°C to +125°C) MB Military tested in accordance with Mil-Std-883-TM5004 (-55°C to +125°C)
			C 8SBDIP
			-2 100KHz/1.8V to 5.5V -3 400KHz/2.5V to 5.5V
			FT24C32 FT24C64

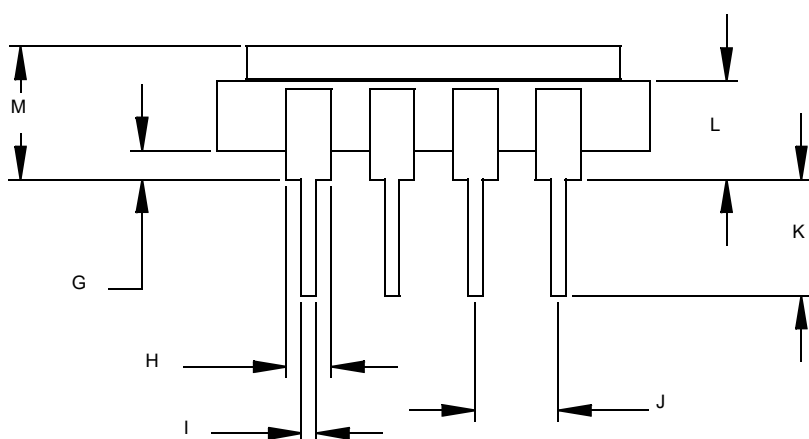
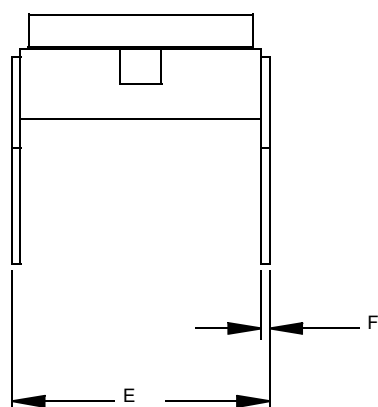
16.1 Package Information

Package Type	
8SBDIP	8-Lead Side Brazed Dual In-Line Package

16.2 8SBDIP



8-SBDIP			
	MIN	NOM	MAX
A			
B			
C	13.01	13.21	13.41
D	7.62	7.87	8.12
E	7.37	7.62	7.87
F	0.45	0.50	0.55
G	0.75	1.00	1.25
H	1.14	1.19	1.24
I	0.43	0.48	0.53
J	2.41	2.54	2.67
K	4.25	4.50	4.75
L	2.68	3.16	3.64
M			
DIMENSIONS IN MILLIMETERS			



28. Force Technologies - B - SCREENING FLOW

The device shall be screened as specified in the table below. Manufactured batches shall have Lots tests carried out in accordance with Mil-Std-883 (Sample size determined by MIL-PRF-38535 Appendix D unless alternatively defined below)

Screening	Method	QA test condition	Sample Size
Internal Visual (Pre-Cap)	Mil-Std-883 TM2010	Cond B	100%
Die Shear	Mil-Std-883 TM2019		Lot Sample
Bond Pull	Mil-Std-883 TM2011		Lot Sample
Temperature Cycle	Mil-Std-883 TM1010	Cond C, 10 Cycles Min	100%
Constant Acceleration	Mil-Std-883 TM2001	Cond E (Min), Y1 Orientation.	100%
Visual Inspect	Review for catastrophic failures		100%
Pre-Burn In Electrical	In accordance with applicable device specification.		100%
Burn In	Mil-Std-883 TM1015	160 hours at +125°C Min	100%
PDA Calculation	5% PDA	Check for burn in Failure rate	Data Review
Final Electrical Test	In accordance with applicable device specification.		100% -55°C T min +25°C +125°C T max
Seal a. Fine Leak b. Gross Leak	Mil-Std-883 TM1014		100%
External Visual	Mil-Std-883 TM2009		100%
Marking & Inspect	As FT WIP documentation	Laser Flow WP1024	100%
Data Preparation	As FT QA documentation	AS9100 Rev D	100%
Dry Bake store/ship	As FT WIP documentation	Bake and Dry WP1033	100%

29. Revision History

Rev	Date	Description
- 1	October 2025	- Original



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