FT27C256R

256K (32K x 8) UVEPROM

1. Feature

- **Fast Read Access Time**
- **Low-Power CMOS Operation**
  - **100 µA max. Standby**
  - **20 mA max.   ctive at 5 MHz**
- **JEDEC Standard Packages**
  - **28-Lead 600-mil Ceramic**
  - **32-Lead Ceramic LCC**
  - **+ Ceramic Custom**
- **5V ± 10% Supply**
- **High Reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Comm, Ind and Mil Temp inc. Mil-Std-883 M5004**

2. Description

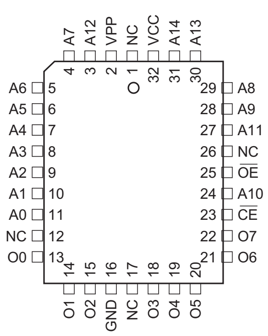
The FT27C256R is a low-power, high-performance 262,144-bit programmable memory organised 32K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

CMOS technology provides low-active power consumption, and fast programming. Power consumption is typically only 8 mA in Active Mode and less than 10 µA in Standby.

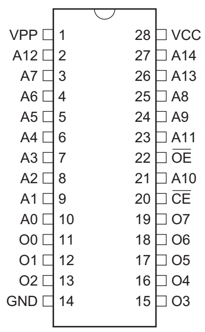
3. Pin Configu ation

Pin Name	Function
A0 - A14	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

LCC



SBDIL



The FT27C256R is available in a choice of industry standard JEDEC-approved windowed packages.
All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flex-ibility to prevent bus contention.

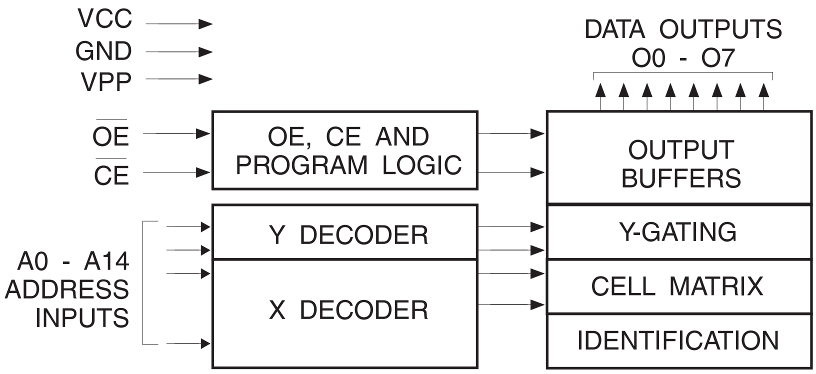
With 32K byte storage capability, the FT27C256R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

The FT27C256R has additional features to ensure high quality and efficient production use. Programing Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilised for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilise the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilised, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



5. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0 volts for pulses of less than 20 ns.

6. Operating Modes

˘ ode\Pin	$\overline{CE}$	$\overline{˘*}$	Ai	3$_{PP}$	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	High Z
Standby	V_{IH}	X(1)	X(1)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM Verify(2)	X(1)	V_{IL}	Ai	V_{PP}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X(1)	V_{PP}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 = V_H(3) A0 = V_{IH} or V_{IL} A1 - A14 = V_{IL}	V_{CC}	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer’s Identification byte and high (V_{IH}) to select the Device Code byte.

7. DC and AC Characteristics for Read Operation

		FT$7C256R					
		-70	-90	-12	-15	-20	-$&
Operating Temp. (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil			-55°C - 125°C	-55°C-125°C	-55°C - 125°C	-55°C -125°C
V_{CC} Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

8. DC Characteristics for Read Operation

ˆ ymbo0	Parameter	Conditio˝	˘ in	˘ a	?˝ its
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	uA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		10	µA
I_{PP1}(2)	V_{PP}(1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC}(1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$= V_{CC} ± 0.3V		100com/200mil	uA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		2com/3mil	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{E}$ = V_{IL}		20com/25mil	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

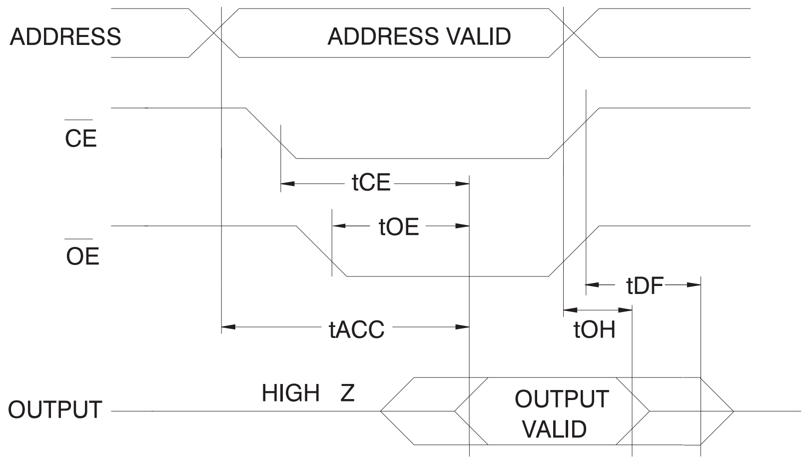
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}

9. AC Characteristics for Read Operation

			FT27C256R												
			-20		-25		-70		-90		-12		-15		
ˆ ymbo0	Parameter	Condition	Min	˘ a	˘ i˝	˘ ax	˘ i˝	˘ ax	Min	˘ a	Min	Ma	˘ i˝	˘ ax	Units
t_{ACC}(3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200		250		70		90		120		150	ns
t_{CE}(2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		200		250		70		90		120		150	ns
t_{OE}(2)(3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		75		100		30		40		50		60	ns
t_{DF}(4)(5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			55		60		30		30		30		45	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first			0		0		0		0		0		0	ns

Note: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

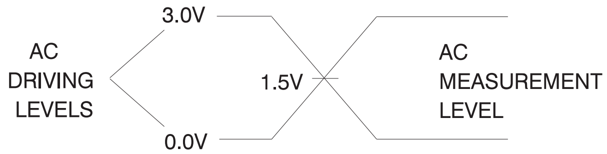
10. AC F aveforms for Read Opesation(1)



Notes:
1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

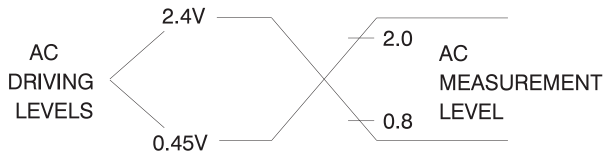
11. Input Test Waveforms and Measurement Levels

For -45 and -55 devices only:



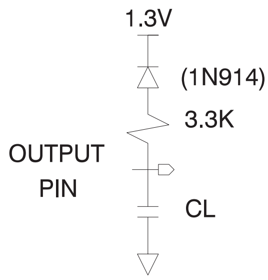
t_R, t_F < 5 ns (10% to 90%)

For -70, -90, -12, and -20 devices:



t_R, t_F < 20 ns (10% to 90%)

12. Output Test Load



Note: C_L = 100 pF including jig capacitance, except for the -45 and -55 devices, where C_L = 30 pF.

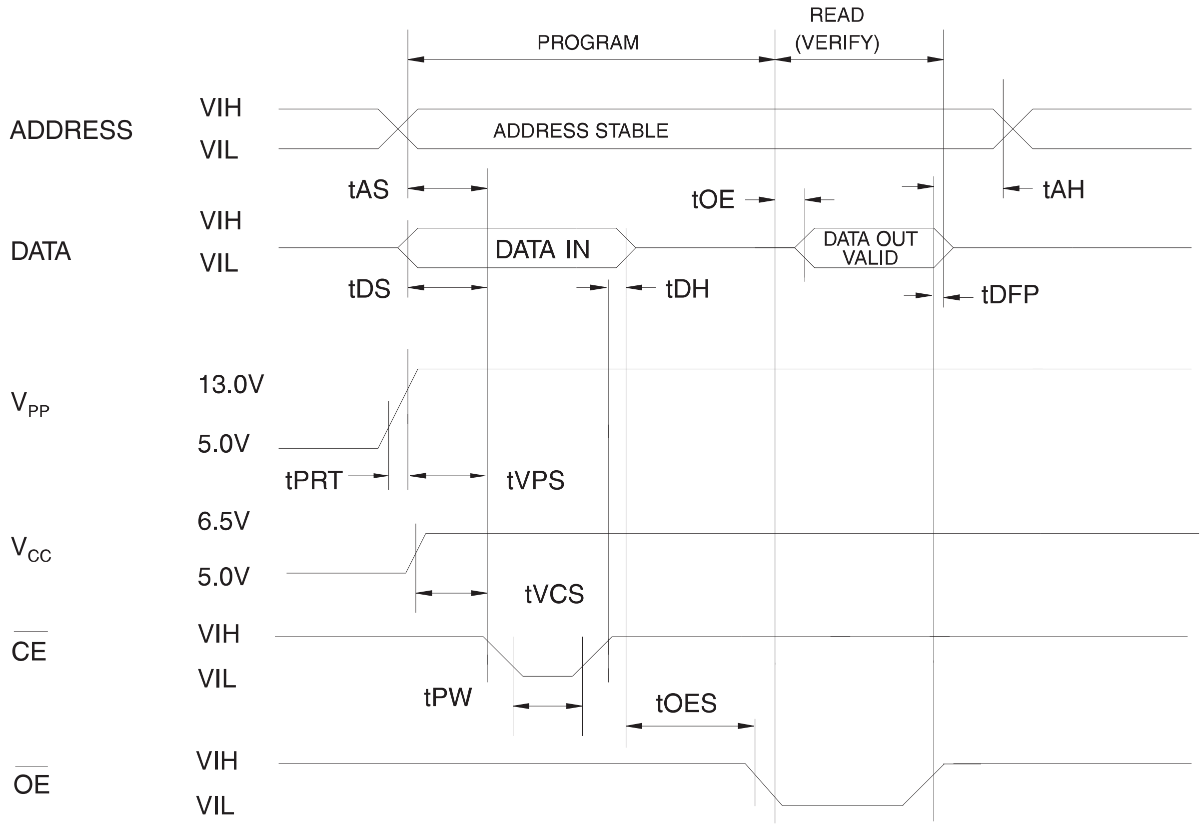
13. Pin Capacitance

f = 1 MHz, T = 25°C(1)

ˆ# mbol	T#˙	˘ a	?˝ its	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

14. Programming Waveforms(1)



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the FT27C256R a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

15. DC Programming Characteriritic

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

ˆ# mbol	Parameter	Test Conditions	Limits Min	Limits ˇ ax	Units
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Volt	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Volt	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

16. AC Programming Characteristic

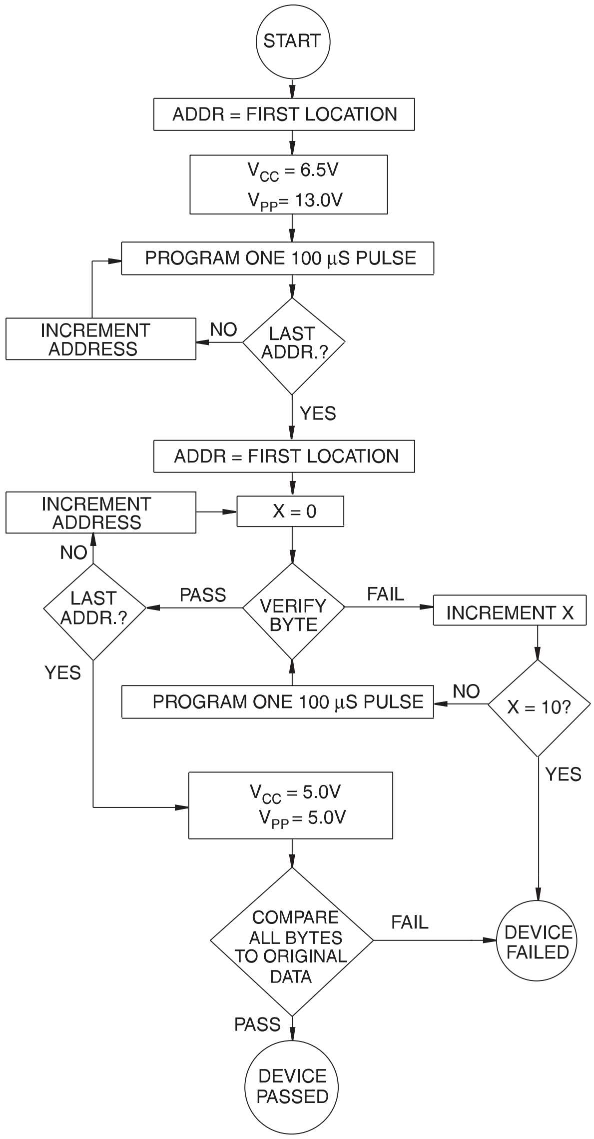
$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $V_{PP} = 13.0 \pm 0.25V$

			Limits		
ˆ# mbol	Parameter	Test Conditions[1]	Mi˝	Ma	Units
t_{AS}	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20ns Input Pulse Levels 0.45V to 2.4V Input Timing Reference Level 0.8V to 2.0V Output Timing Reference Level 0.8V to 2.0V	2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay[2]		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width[3]		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$[2]			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

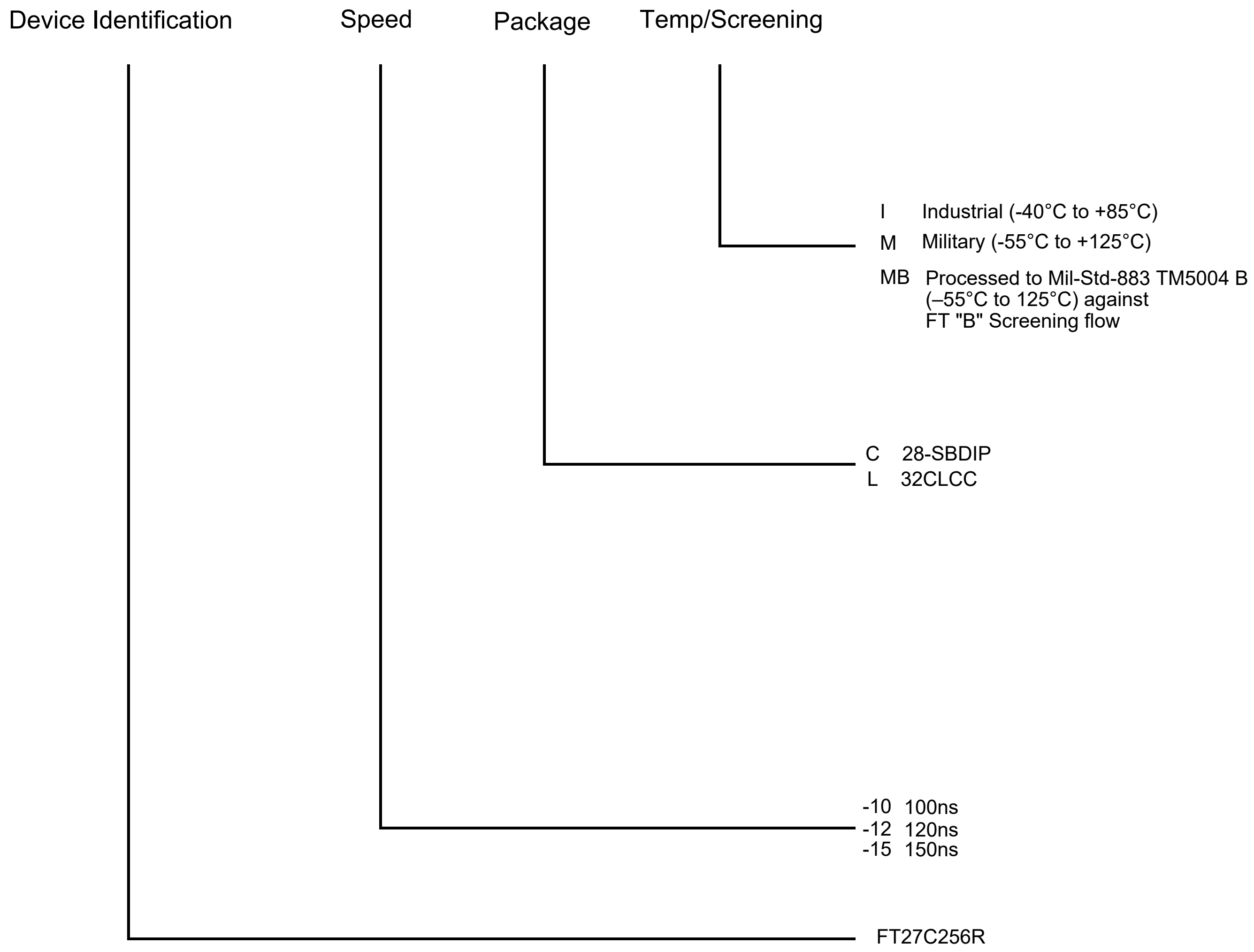
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

17. Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



27. Ordering Information

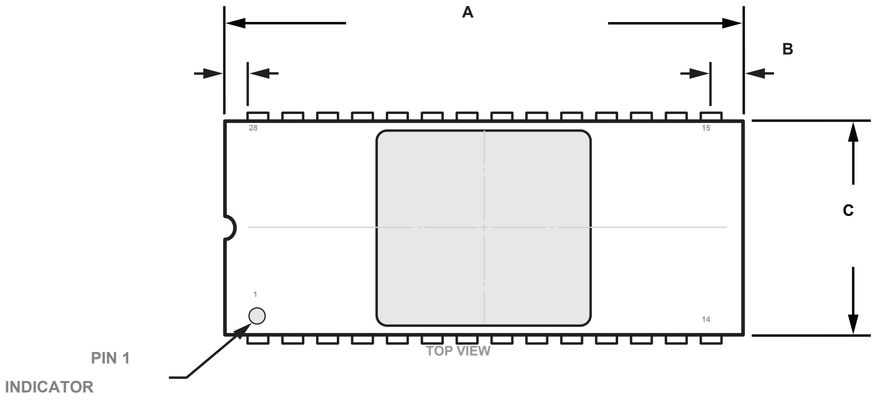


27.1 Package Information

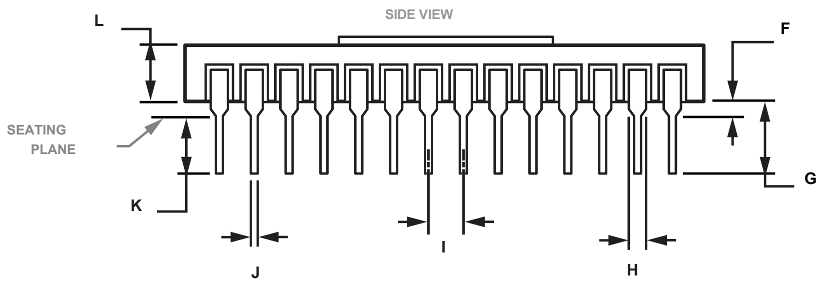
Package Type	
28SBDIP	28-lead, Ceramic Side Brazed Dual In-Line Package
32CLCC	32-Pad, Non-windowed, Ceramic Leadless Chip Carrier

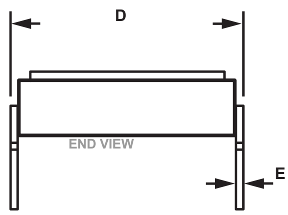
*Additional packages available upon request

20.1.1 28SBDIP

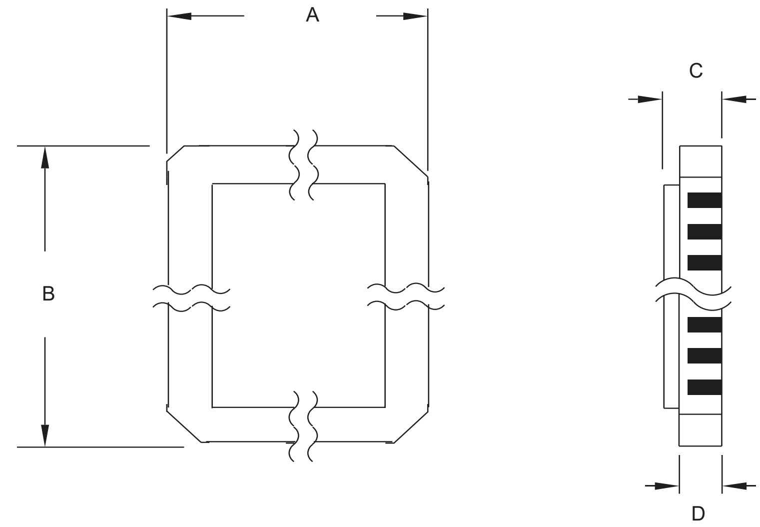


28SBDIP			
	MIN	NOM	MAX
A	1.260	1.400	1.540
B	0.030	0.050	0.070
C	0.585	0.595	0.605
D	0.600	0.610	0.620
E	0.008	0.010	0.012
F	0.060	0.050	0.060
G	0.056	0.068	0.080
H	0.050 TYP		
I	0.095	0.100	0.105
J	0.016	0.018	0.020
K	0.016	0.018	0.020
L	0.076	0.085	0.094
DIMENSIONS IN INCHES			

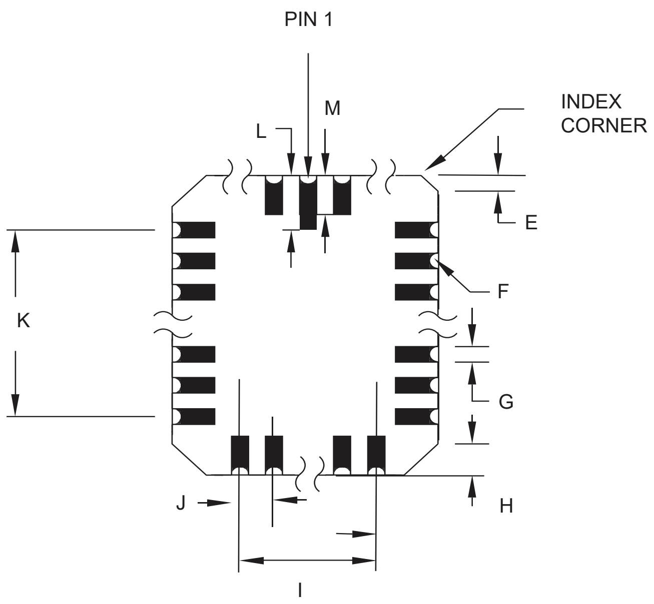




20.1.2 32CLCC



FT32CLCC			
	MIN	NOM	MAX
A	11.30	11.43	11.56
B	13.82	13.97	14.12
C			
D	1.60	1.78	1.96
E	C0.50		
F	R0.23		
G	0.56	0.64	0.72
H	C1.00		
I	7.49	7.62	7.75
J	1.27 TYP		
K	10.03	10.16	10.29
L	1.96	2.16	2.36
M	1.14	1.27	1.40
MILLIMETERS			



21. Force Technologies - B - SCREENING FLOW

The device shall be screened as specified in the table below. Manufactured batches shall have Lots tests carried out in accordance with Mil-Std-883 (Sample size determined by MIL-PRF-38535 Appendix D unless alternatively defined below)

Screening	Method	QA test condition	Sample Size
Internal Visual (Pre-Cap)	Mil-Std-883 TM2010	Cond B	100%
Die Shear	Mil-Std-883 TM2019		Lot Sample
Bond Pull	Mil-Std-883 TM2011		Lot Sample
Temperature Cycle	Mil-Std-883 TM1010	Cond C, 10 Cycles Min	100%
Constant Acceleration	Mil-Std-883 TM2001	Cond E (Min), Y1 Orientation.	100%
Visual Inspect	Review for catastrophic failures		100%
Pre-Burn In Electrical	In accordance with applicable device specification.		100%
Burn In	Mil-Std-883 TM1015	160 hours at +125°C Min	100%
PDA Calculation	5% PDA	Check for burn in Failure rate	Data Review
Final Electrical Test	In accordance with applicable device specification.		100% -55°C T min +25°C +125°C T max
Seal a. Fine Leak b. Gross Leak	Mil-Std-883 TM1014		100%
External Visual	Mil-Std-883 TM2009		100%
Marking & Inspect	As FT WIP documentation	Laser Flow WP1024	100%
Data Preparation	As FT QA documentation	AS9100 Rev D	100%
Dry Bake store/ship	As FT WIP documentation	Bake and Dry WP1033	100%

22. Revision History

Rev	Date	Description
- 1	2007	- Original
- 1.1	2007	- 200/250ns Speed Information Added
- 1.2	February 2012	- Image Quality Increased
- 1.3	July 2012	- MSL Levels Added
- 1.4	March 2013	- 90ns Removed
- 2	October 2025	- Removed Plastic Packages - Updated Package Drawings - Added Screening Table - Format Changes

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