FT28C64B

64K (8K x 8) EEPROM with Page Write and Software Data Protection

Features

- **Fast Read Access Time – 150 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 10 ms Maximum**
  - **1 to 64-byte Page Write Operation**
- **Low Power Dissipation**
  - **40 mA Active Current**
  - **100 µ A CMOS Standby Current**
- **Hardware and Software Data Protection**
- **DATA Polling and Toggle Bit for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 10 Years**
- **Single 5V ±10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-wide Pinout**
- **Industrial & Military Temperature Ranges**

1. Description

The FT28C64B is a high-performance electrically-erasable and programmable read-only memory (EEPROM). Its 64K of memory is organised as 8,192 words by 8 bits. Manufactured with advanced non-volatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

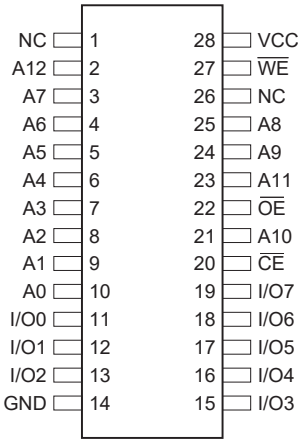
The FT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The FT28C64B has additional features to ensure high quality and manufacturability. The device utilities internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

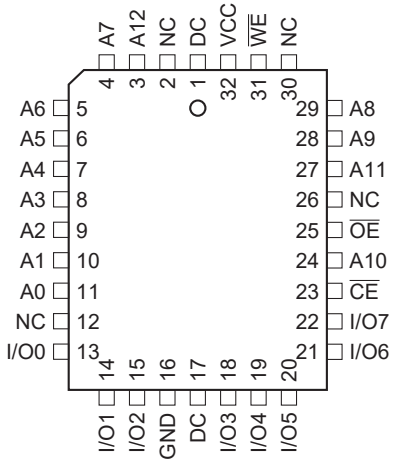
2. Pin Configurations

Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

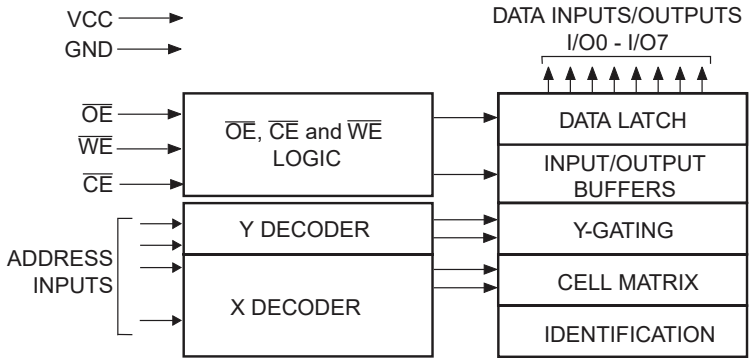
2.1 28-lead SBDIP



2.2 32-lead PLCC



3. Block Diagram



4. Device Operation

4.1 Read

The FT28C64B is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

4.2 Byte Write

A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

4.3 Page Write

The page write operation of the FT28C64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the FT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

4.4 $\overline{\text{DATA}}$ Polling

The FT28C64B features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at any time during the write cycle.

4.5 Toggle Bit

In addition to $\overline{\text{DATA}}$ Polling, the FT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

4.6 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. The FT28C64B has both hardware and software features that will protect the memory against inadvertent writes.

4.6.1 Hardware Data Protection

Hardware features protect against inadvertent writes to the FT28C64B in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8 V (typical), the write function is inhibited; (b) V_{CC} power-on delay – once V_{CC} has reached 3.8 V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high, or $\overline{\text{WE}}$ high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

4.6.2 Software Data Protection

A software controlled data protection feature has been implemented on the FT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the FT28C64B is shipped from Force with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (see “Software Data Protection Algorithms” on page 10). After writing the 3-byte command sequence and waiting t_{WC}, the entire FT28C64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the FT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the FT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of t_{WC}, read operations will effectively be polling operations.

4.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

5. DC and AC Operating Range

	FT28C64B-15 (Mil)	FT28C64B-15 (Ind)
Operating Temperature (Case)	-55°C - 125°C	-40°C - 85°C
V_{CC} Power Supply	5V ±10%	5V ±10%

6. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H(3)	V_{IL}	High Z

Notes:
1. X can be V_{IL} or V_{IH}.
2. See “AC Write Waveforms” on page 8.
3. V_H = 12.0V ±0.5V.

7. Absolute Maximum Ratings*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages (including NC Pins) with Respect to Ground .....-0.6V to +6.25V

All Output Voltages with Respect to Ground .....-0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9 with Respect to Ground .....-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

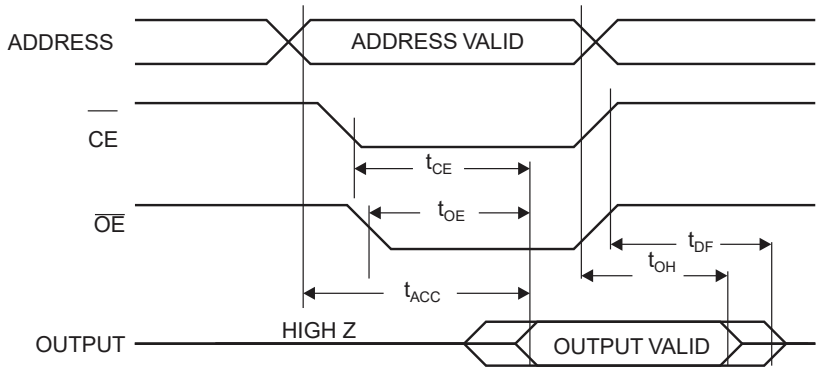
8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		2	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.40	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

9. AC Read Characteristics

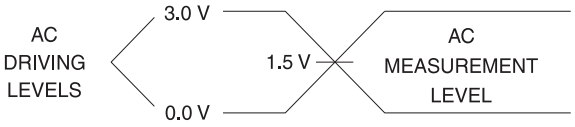
Symbol	Parameter	FT28C64B-15		Units
		Min	Max	
t_{ACC}	Address to Output Delay		150	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		150	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	70	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

10. AC Read Waveforms[1][2][3][4]



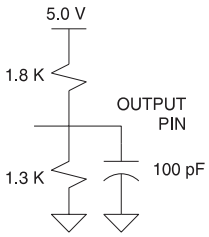
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterised and is not 100% tested.

11. Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

12. Output Test Load



13. Pin Capacitance

f = 1 MHz, T = 25°C(1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

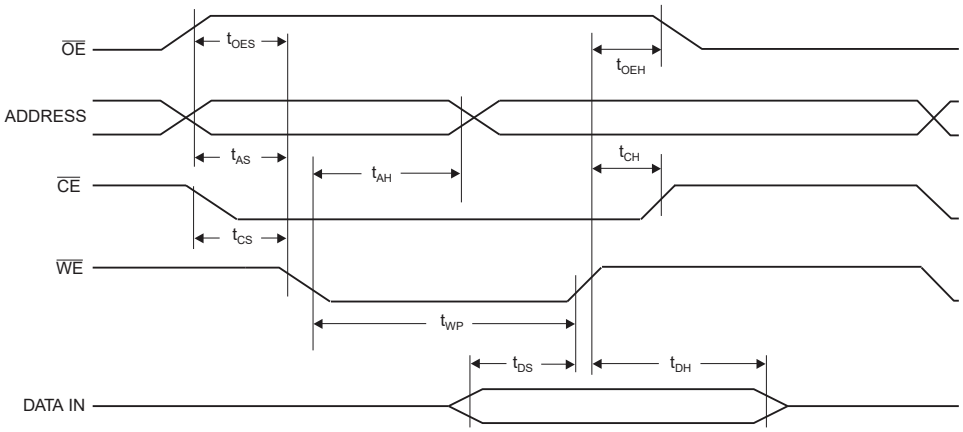
Note: 1. This parameter is characterised and is not 100% tested.

14. AC Write Characteristics

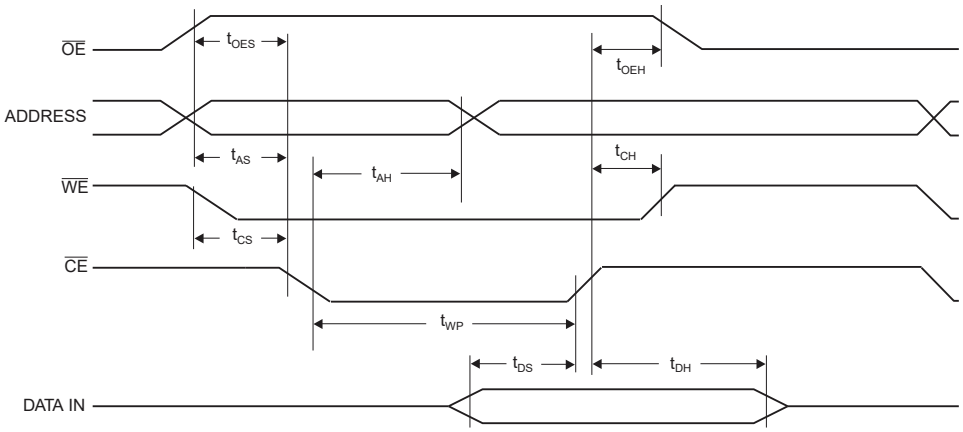
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

15. AC Write Waveforms

15.1 $\overline{WE}$ Controlled



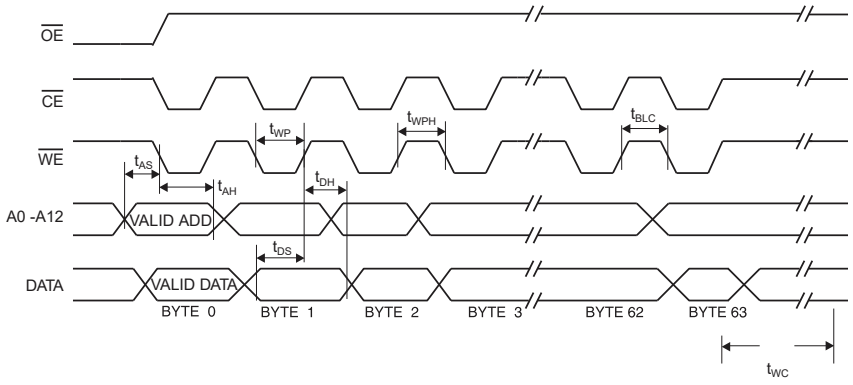
15.2 $\overline{CE}$ Controlled



16. Page Mode Characteristics

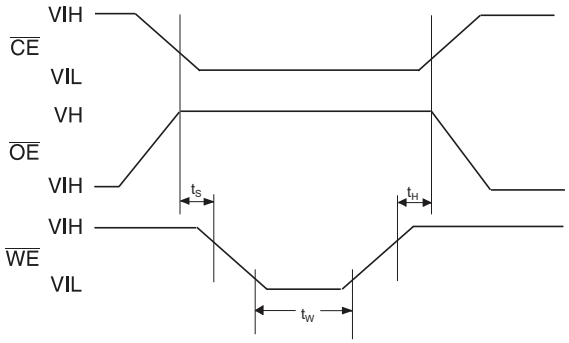
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

17. Page Mode Write Waveforms(1)(2)



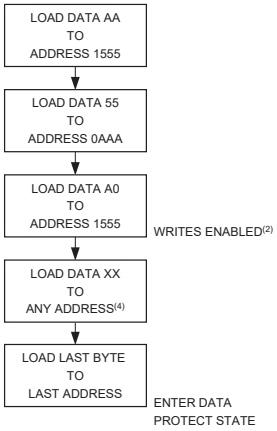
Notes: 1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

18. Chip Erase Waveforms



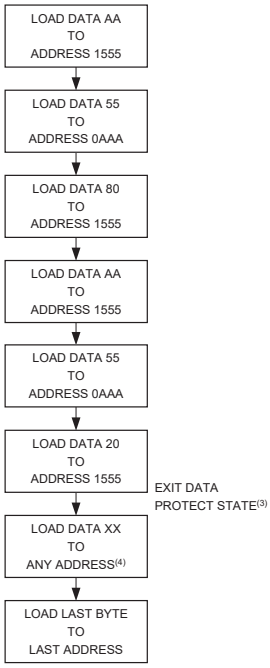
$t_S = t_H = 1$ µs (min.)
$t_W = 10$ ms (min.)
$V_H = 12.0V \pm 0.5V$

19. Software Data Protection Enable Algorithm(1)



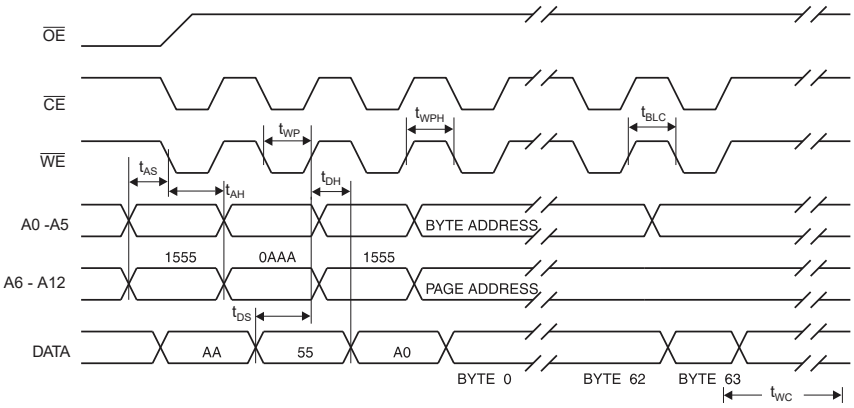
Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

20. Software Data Protection Disable Algorithm(1)



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A12 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

21. Software Protected Write Cycle Waveforms(1)(2)



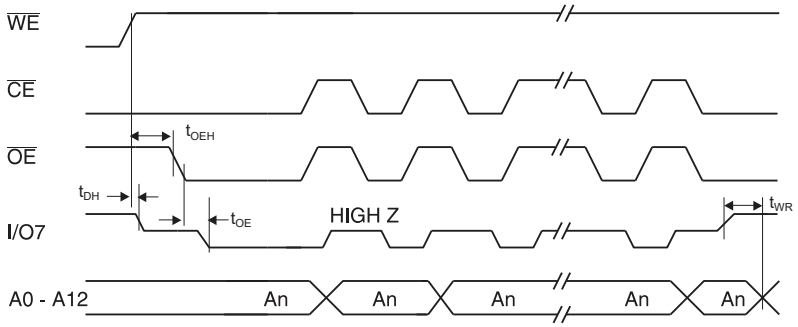
Notes:
1. A6 through A12 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

22. $\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay(1)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterised and not 100% tested. See “AC Read Characteristics” on page 6.

23. $\overline{\text{Data}}$ Polling Waveforms

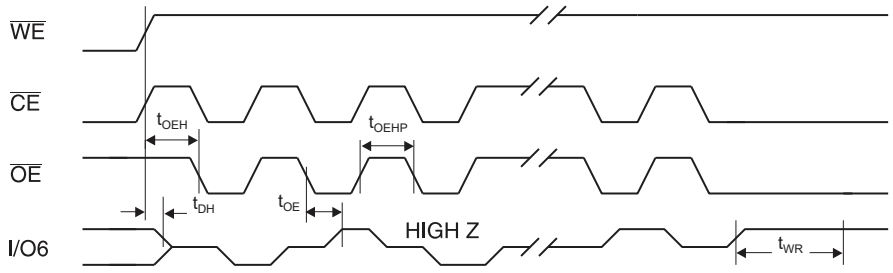


24. Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterised and not 100% tested.
2. See “AC Read Characteristics” on page 6.

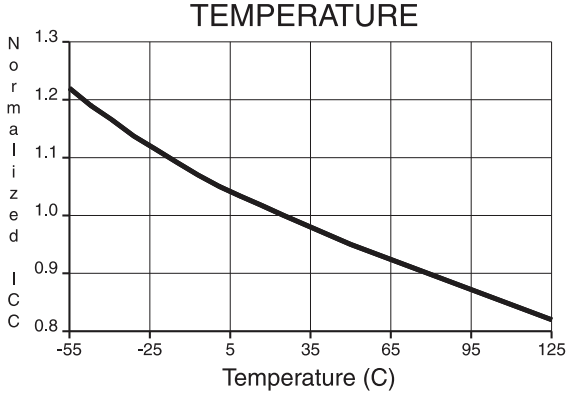
25. Toggle Bit Waveforms(1)(2)(3)



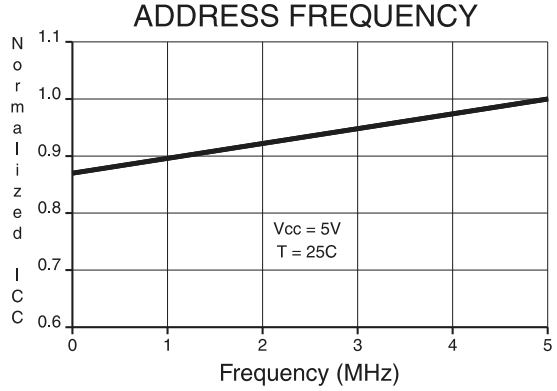
Notes: 1. Toggling either OE or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

26. Normalised I_{CC} Graphs

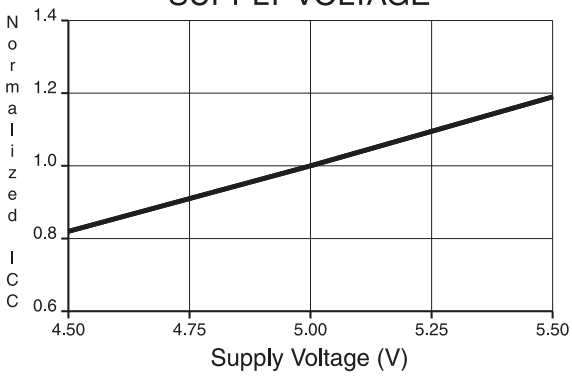
NORMALISED SUPPLY CURRENT vs. TEMPERATURE



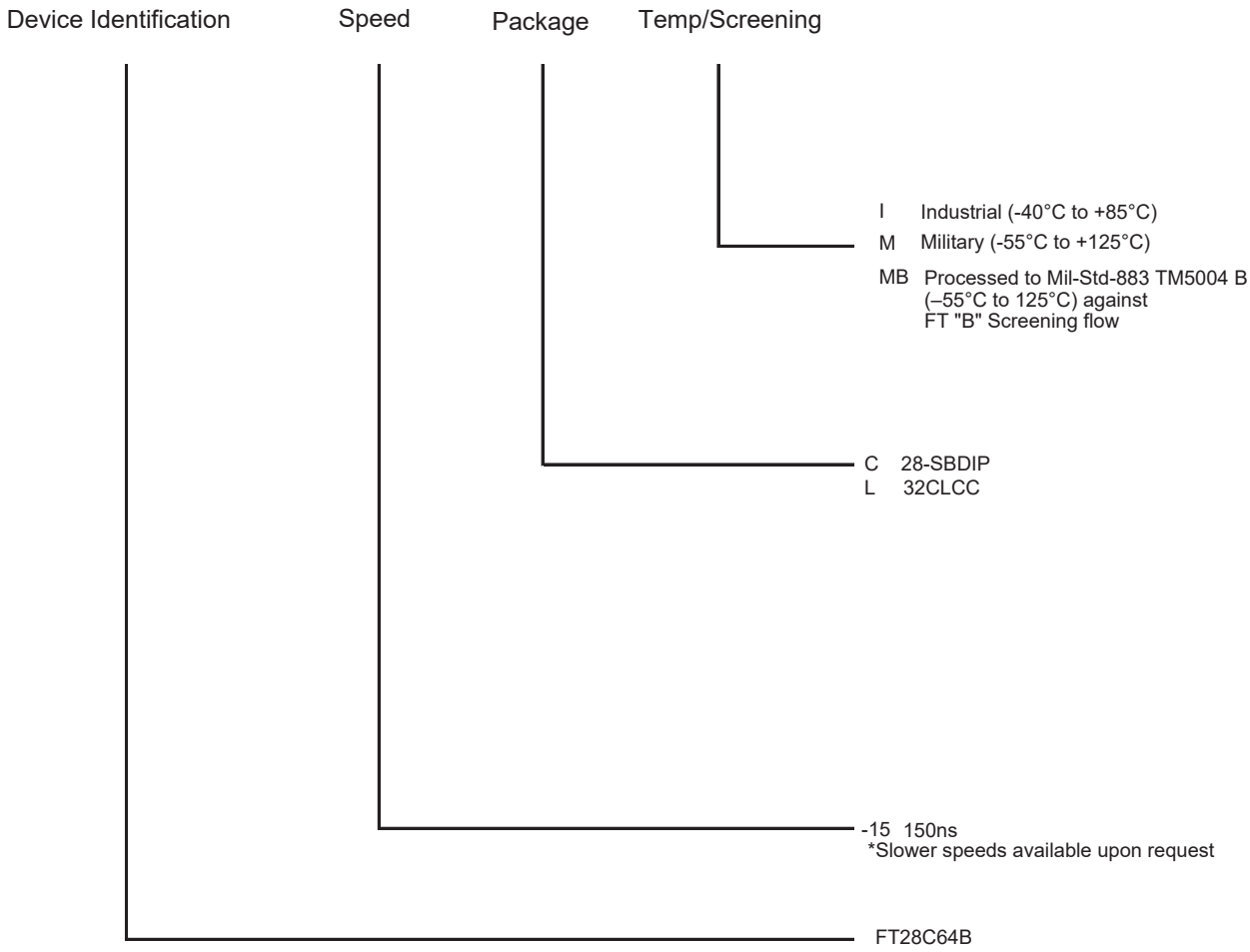
NORMALISED SUPPLY CURRENT vs. ADDRESS FREQUENCY



NORMALISED SUPPLY CURRENT vs. SUPPLY VOLTAGE



27. Ordering Information

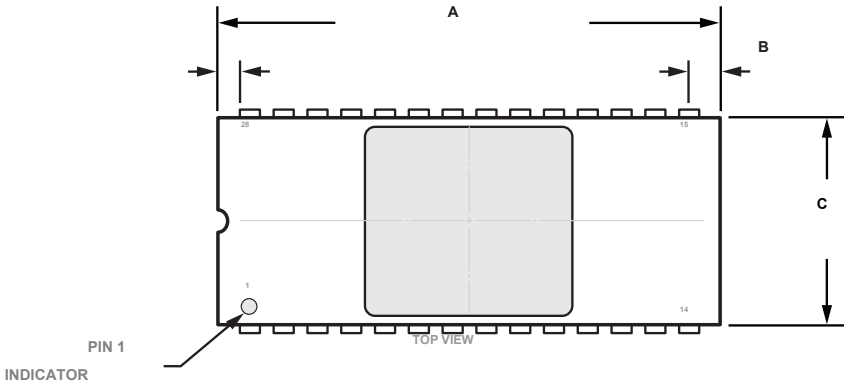


27.1 Packaging Information

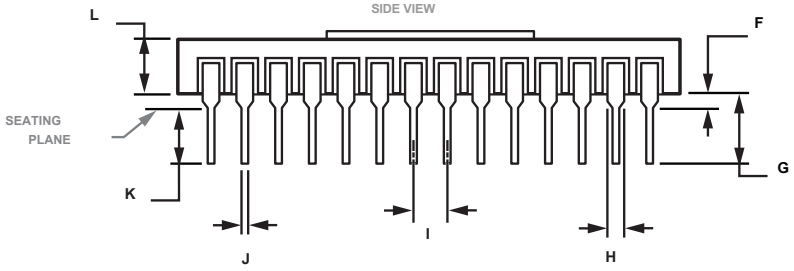
Package Type	
28SBDIP	28-lead, Ceramic Side Brazed Dual In-Line Package
32CLCC	32-Pad, Non-windowed, Ceramic Leadless Chip Carrier

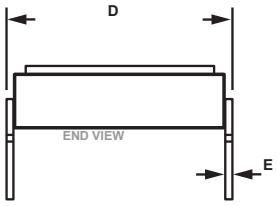
*Additional packages available upon request

27.2 28SBDIP

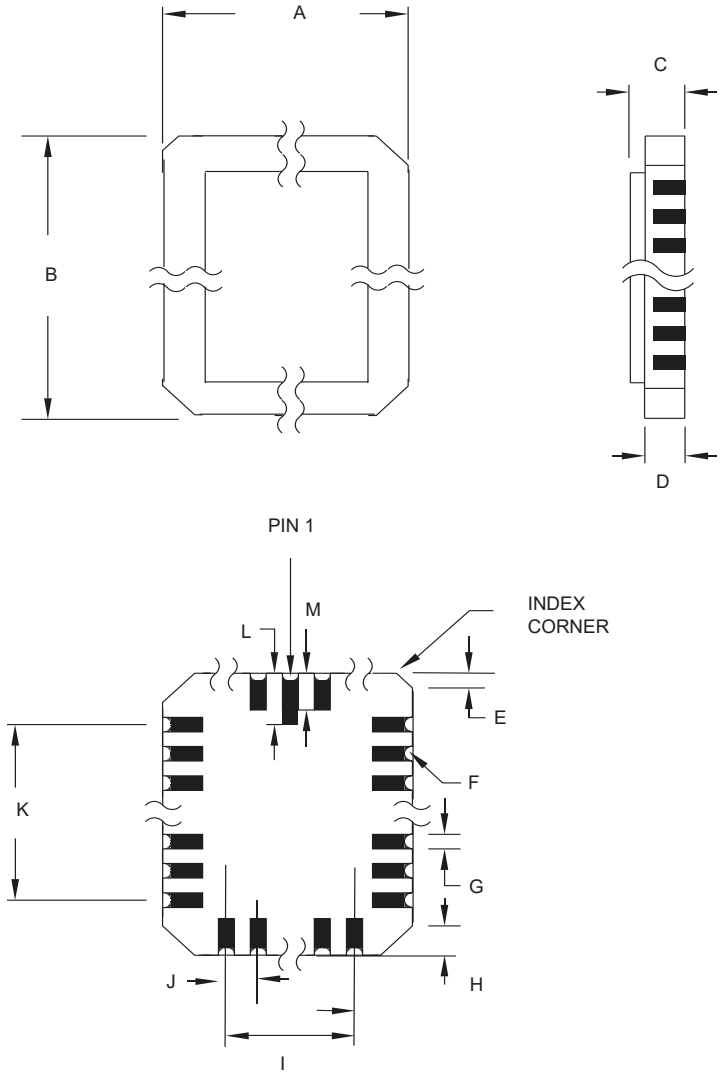


28SBDIP			
	MIN	NOM	MAX
A	1.260	1.400	1.540
B	0.030	0.050	0.070
C	0.585	0.595	0.605
D	0.600	0.610	0.620
E	0.008	0.010	0.012
F	0.060	0.050	0.060
G	0.056	0.068	0.080
H	0.050 TYP		
I	0.095	0.100	0.105
J	0.016	0.018	0.020
K	0.016	0.018	0.020
L	0.076	0.085	0.094
DIMENSIONS IN INCHES			





27.1.2 32CLCC



FT32CLCC			
	MIN	NOM	MAX
A	11.30	11.43	11.56
B	13.82	13.97	14.12
C			
D	1.60	1.78	1.96
E	C0.50		
F	R0.23		
G	0.56	0.64	0.72
H	C1.00		
I	7.49	7.62	7.75
J	1.27 TYP		
K	10.03	10.16	10.29
L	1.96	2.16	2.36
M	1.14	1.27	1.40
MILLIMETERS			

28. Force Technologies - B - SCREENING FLOW

The device shall be screened as specified in the table below. Manufactured batches shall have Lots tests carried out in accordance with Mil-Std-883 (Sample size determined by MIL-PRF-38535 Appendix D unless alternatively defined below)

Screening	Method	QA test condition	Sample Size
Internal Visual (Pre-Cap)	Mil-Std-883 TM2010	Cond B	100%
Die Shear	Mil-Std-883 TM2019		Lot Sample
Bond Pull	Mil-Std-883 TM2011		Lot Sample
Temperature Cycle	Mil-Std-883 TM1010	Cond C, 10 Cycles Min	100%
Constant Acceleration	Mil-Std-883 TM2001	Cond E (Min), Y1 Orientation.	100%
Visual Inspect	Review for catastrophic failures		100%
Pre-Burn In Electrical	In accordance with applicable device specification.		100%
Burn In	Mil-Std-883 TM1015	160 hours at +125°C Min	100%
PDA Calculation	5% PDA	Check for burn in Failure rate	Data Review
Final Electrical Test	In accordance with applicable device specification.		100% -55°C T min +25°C +125°C T max
Seal a. Fine Leak b. Gross Leak	Mil-Std-883 TM1014		100%
External Visual	Mil-Std-883 TM2009		100%
Marking & Inspect	As FT WIP documentation	Laser Flow WP1024	100%
Data Preparation	As FT QA documentation	AS9100 Rev D	100%
Dry Bake store/ship	As FT WIP documentation	Bake and Dry WP1033	100%

29. Revision History

Rev	Date	Description
- 1	2010	- Original
- 2	October 2025	- Package Changes - Updated Package Drawings - Added Screening Table - Format Changes

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