Features

- **Read Access Time – 200 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 256 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Time**
  - **Page Write Cycle Time – 10 ms Maximum**
  - **1 to 256 Byte Page Write Operation**
- **Low Power Dissipation**
  - **50 mA Active Current**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10,000 Cycles**
  - **Data Retention: 10 Years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**

4-Megabit (512K x 8) Paged Parallel EEPROMs

FT28C040

1. Description

The FT28C040 is a high-performance electrically erasable and programmable read-only memory (EEPROM). Its 4 megabits of memory is organised as 524,288 words by 8 bits. Manufactured with advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 440 mW.

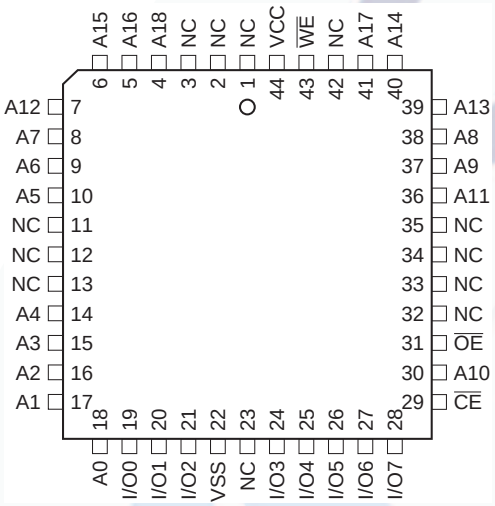
The FT28C040 is accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 256-byte page register to allow writing of up to 256 bytes simultaneously. During a write cycle, the address and 1 to 256 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{Data}}$ Polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Force's FT28C040 has additional features to ensure high quality and manufacturability. The device utilises internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 256 bytes of EEPROM for device identification or tracking.

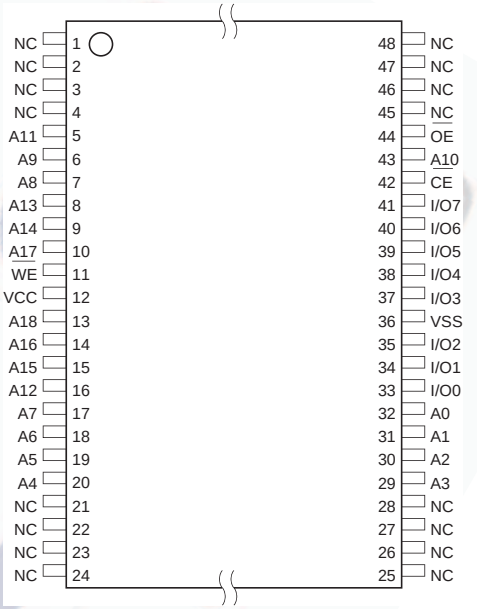
2. Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

2.1 44-lead LCC – Top View



2.2 48-lead CFP – Top View



2.3 32-lead Side Braze, Flatpack – Top View