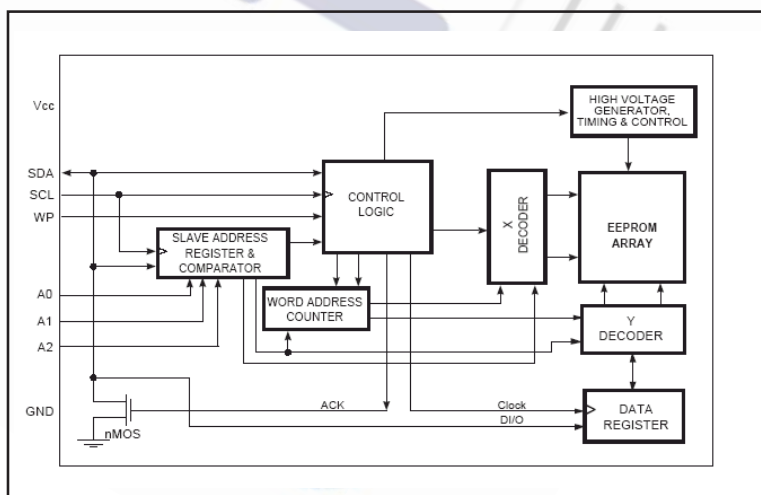


### Description

The FTE24C32A/B and FTE24C64A/B are electrically erasable PROM devices that use the standard 2-wire interface for communications. The FTE24C32A/B and FTE24C64A/B contain a memory array of 32K-bits (4Kx8) and 64K-bits (8Kx8) respectively, and each is further subdivided into 32 byte pages for Page-Write mode. This EEPROM is offered in wide operating voltages of 2.5V to 5.5V to be compatible with most application voltages. Force Technologies designed the FTE24C32A/B and FTE24C64A/B to be a practical, low-power 2-wire EEPROM solution. The devices are packaged in 8-pin Ceramic DIP, Flatpack, 20 Pin LCC and 8 pin Plastic DIP or SOIC.

The FTE24C32A/B and FTE24C64A/B maintain compatibility with the popular 2-wire bus protocol, so it is easy to design into applications implementing this bus type. The simple bus consists of the Serial Clock wire (SCL) and the Serial Data wire (SDA). Using the bus, a Master device such as a microcontroller is usually connected to one or more Slave devices such as the FTE24C32A/B and FTE24C64A/B. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The FTE24C32A/B and FTE24C64A/B has a Write Protect pin (WP) to allow blocking of any write instruction transmitted over the bus.

- Two-Wire Serial Interface, I<sup>2</sup>C™ compatible Bi-directional data transfer protocol
- 400 KHz (2.5V) and 1 MHz (5.0V) compatibility
- Low Power CMOS Technology
  - Active Current less than 3 mA (5.0V)
  - Standby Current less than 6 µA (5.0V)
  - Standby Current less than 2 µA (2.5V)
- Wide Voltage Operation
  - V<sub>cc</sub> = 2.5V to 5.5V
- Hardware Data Protection
  - Write Protect Pin
- Sequential Read Feature
- Filtered Inputs for Noise Suppression
- Hardware Data Protection
  - FTE24C32A/64A: WP protects entire array
  - FTE24C32B/64B: WP protects top quarter of array
- Self time write cycle with auto clear
  - 5 ms @ 5.0V
- Organisation:
  - 24C32: 4Kx8 (128 pages of 32 bytes)
  - 24C64: 8Kx8 (256 pages of 32 bytes)
- 32 Byte Page Write Buffer
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 40 Years
- Military and Extended temperature ranges



Function Block Diagram

Pin Name	DIP, SOIC, Flat Pack 8 Pin Package	LCC20 Pkg
A0	1	5
A1	2	6
A2	3	7
GND	4	10
SDA	5	15
SCL	6	16
WP	7	17
VCC	8	20

Table 1. Pin Configurations

## PIN DESCRIPTIONS

A0-A2	Address Inputs
SDA	Serial Address/Data I/O
SCL	Serial Clock Input
WP	Write Protect Input
Vcc	Power Supply
GND	Ground

### SCL

This input clock pin is used to synchronise the data transfer to and from the device.

### SDA

The SDA is a Bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wire-Or'ed with other open drain or open collector outputs. The SDA bus requires a pullup resistor to Vcc.

### A0, A1, A2

The A0, A1 and A2 are the device address inputs that are hardwired or left not connected for hardware compatibility with the 24C16. When pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system. When the pins are not hardwired, the default values of A0, A1, and A2 are zero.

### WP

WP is the Write Protect pin. The input level determines if all, or none of the array is protected from modifications.

## DEVICE OPERATION

The FTE24C32A/B and FTE24C64A/B feature serial communication and support a bi-directional 2-wire bus transmission protocol called I<sup>2</sup>C™.

### 2-WIRE BUS

The two-wire bus is defined as a Serial Data line (SDA), and a Serial Clock line (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers.

The bus is controlled by Master device which generates the SCL, controls the bus access and generates the Stop and Start conditions. The FTE24C32A/B and FTE24C64A/B are the Slave device on the bus.

### The Bus Protocol:

- Data transfer may be initiated only when the bus is not busy
- During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the data line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition.

### Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The FTE24C32A/B and FTE24C64A/B monitors the SDA and SCL lines and will not respond until the Start condition is met.

### Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

### Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

### Reset

The FTE24C32A/B and FTE24C64A/B contains a reset function in case the 2-wire bus transmission is accidentally interrupted (eg. a power loss), or needs to be terminated mid-stream. The reset is caused when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

### Standby Mode

Power consumption is reduced in standby mode. The FTE24C32A/B and FTE24C64A/B will enter standby mode:

- a) At Power-up, and remain in it until SCL or SDA toggles;
- b) Following the Stop signal if no write operation is initiated; or c) Following any internal write operation

### DEVICE ADDRESSING

The Master begins a transmission by sending a Start condition. The Master then sends the address of the particular Slave devices it is requesting. The Slave device (Fig. 5) address is 8 bits. The four most significant bits of the Slave device address are fixed as 1010 for the FTE24C32A/B and FTE24C64A/B.

This device has three address bits (A2, A1, and A0), which allows up to eight FTE24C32A/B and FTE24C64A/B devices to share the 2-wire bus. Upon receiving the Slave address, the device compares the three address bits with the hardwired A2, A1, and A0 input pins to determine if it is the appropriate Slave.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master transmits the Start condition and Slave address byte (Fig. 5), the appropriate 2-wire Slave (eg. FTE24C32/FTE24C64) will respond with ACK on the SDA line. The Slave will pull down the SDA on the ninth clock cycle, signaling that it received the

eight bits of data. The selected FTE24C32A/B and FTE24C64A/B then prepares for a Read or Write operation by monitoring the bus.

### WRITE OPERATION

#### Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the two byte address that are to be written into the address pointer of the FTE24C32A/B and FTE24C64A/B. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The FTE24C32A/B and FTE24C64A/B acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

#### Page Write

The FTE24C32A/B and FTE24C64A/B is capable of 32-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 31 more bytes. After the receipt of each data word, the FTE24C32A/B and FTE24C64A/B responds immediately with an ACK on SDA line, and the five lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 32 words prior to issuing the Stop condition, the address counter will "roll over," and the previously written data will be overwritten. Once all 32 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the FTE24C32A/B and FTE24C64A/B in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.



## Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the FTE24C32A/B and FTE24C64A/B initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the FTE24C32A/B and FTE24C64A/B is still busy with the Write operation, no ACK will be returned. If the FTE24C32A/B and FTE24C64A/B has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

## READ OPERATION

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to "1". There are three Read operation options: current address read, random address read, and sequential read.

### Current Address Read

The FTE24C32A/B and FTE24C64A/B contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location  $n$ , the internal address counter would increment to address location  $n+1$ . When the FTE24C32/FTE24C64 receives the Slave Device Addressing Byte with a Read operation (R/W bit set to "1"), it will respond an ACK and transmit the 8-bit data word stored at address location  $n+1$ . The Master should not acknowledge the transfer but should generate a Stop condition so the FTE24C32/FTE24C64 discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

### Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and word address of the location it wishes to read. After the

FTE24C32A/B and FTE24C64A/B acknowledges the word address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The FTE24C32/FTE24C64 then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

### Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the FTE24C32A/B and FTE24C64A/B sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the FTE24C32A/B and FTE24C64A/B. The FTE24C32/FTE24C64 continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from address  $n+1$ , ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of 8191 for FTE24C64A/B or 4095 for FTE24C32A/B is reached, the address counter "rolls over" to address 0, and the FTE24C32A/B and FTE24C64A/B continues to output data for each ACK received. (Refer to Figure 10. Sequential Read Operation Starting with a Random Address Read Diagram.)

**Absolute Maximum Ratings<sup>1</sup> ( $T_A = 25^\circ\text{C}$ )**

Supply Voltage ( $V_S$ )	+0.5 to +6.5 V	Storage Temperature ( $T_{STG}$ )	-65 to +200°C
Voltage on Any Pin ( $V_P$ )	-0.5 to $V_{CC} + 0.5$ V	Output Current ( $I_{OUT}$ )	5 mA
Temperature UnderBias ( $T_{BIAS}$ )	-55 to +175 °C		

1. Stresses violating the conditions listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device outside these conditions or those indicated in the operational sections of this specification is not implied. Exposure to these conditions for extended periods may affect reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Military	$V_{CC}$	-55 °C to +125 °C	2.5		5.5	V
Extended Temp	$V_{CC}$	-55 °C to +175 °C	4.5		5.5	V

**Capacitance<sup>1,2</sup>**

Parameter	Symbol	Conditions	Max	Units
Input Capacitance	$C_{IN}$	$V_{IN} = 0V$	6	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0V$	8	pF

1. Tested initially and after any design or process changes that may affect these parameters.  
2. Test conditions:  $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{CC} = 5.0V$ .

AC Electrical Characteristics ( $T_A = -55^{\circ}\text{C}$ to $+175^{\circ}\text{C}$ )							
Parameter	Symbol	2.5V-5.5V		4.5V-5.5V <sup>1</sup>		Units	
		Min	Max	Min	Max		
SCL Clock Frequency	$f_{\text{SCL}}$	0	400	0	1000	KHz	
Noise Suppression Time <sup>1</sup>	T	—	50	—	50	ns	
Clock Low Period	$t_{\text{LOW}}$	1.2	—	0.6	—	$\mu\text{s}$	
Clock High Period	$t_{\text{HIGH}}$	0.6	—	0.4	—	$\mu\text{s}$	
Bus Free Time Before New Transmission <sup>1</sup>	$t_{\text{BUF}}$	1.2	—	0.5	—	$\mu\text{s}$	
Start Condition Setup Time	$t_{\text{SU:STA}}$	0.6	—	0.25	—	$\mu\text{s}$	
Stop Condition Setup Time	$t_{\text{SU:STO}}$	0.6	—	0.25	—	$\mu\text{s}$	
Start Condition Hold Time	$t_{\text{HD:STA}}$	0.6	—	0.25	—	$\mu\text{s}$	
Stop Condition Hold Time	$t_{\text{HD:STO}}$	0.6	—	0.25	—	$\mu\text{s}$	
Data In Setup Time	$t_{\text{SU:DAT}}$	100	—	100	—	ns	
Data In Hold Time	$t_{\text{HD:DAT}}$	0	—	0	—	ns	
WP pin Setup Time	$t_{\text{SU:WP}}$	0.6	—	0.6	—	$\mu\text{s}$	
WP pin Hold Time	$t_{\text{HD:WP}}$	1.2	—	1.2	—	$\mu\text{s}$	
Data Out Hold Time (SLC Low to SDA Data Out Change)	$t_{\text{DH}}$	50	—	50	—	ns	
Clock to Out put (SCL Low to SDA Data Out Valid)	$t_{\text{AA}}$	50	900	50	550	ns	
SCL and SDA Rise Time <sup>1</sup>	$t_{\text{R}}$	—	300	—	300	ns	
SCL and SDA Fall Time <sup>1</sup>	$t_{\text{F}}$	—	300	—	100	ns	
Write Cycle Time	$t_{\text{WR}}$	—	10	—	5	ms	

1. This parameter is characterised but not 100% tested.

**DC Electrical Characteristics (TA = -55°C to +175°C)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	$V_{OL}$	$V_{CC} = 2.5V, I_{OL} = 3 \text{ mA}$	—	—	0.4	V
Input High Voltage	$V_{IH}$		$V_{CC} \times 0.7$		$V_{CC} + .05$	V
Input Low Voltage	$V_{IL}$		-1.0		$V_{CC} \times 0.3$	V
Input Leakage Current	$I_{II}$	$V_{IN} = 0V \text{ to } V_{CC}$	—	—	20	$\mu\text{A}$
Output Leakage Current	$I_{LO}$		-20	—	20	$\mu\text{A}$

**Power Supply Characteristics (TA = -55°C to +125°C)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCC Operating Current	$I_{CC1}$	Read at 400 KHz ( $V_{CC} = 5V$ )	—	—	2.0	mA
VCC Operating Current	$I_{CC2}$	Write at 400 KHz ( $V_{CC} = 5V$ )	—	—	3.0	mA
Standby Current	$I_{SB1}$	$V_{CC} = 2.5V$	—	—	2	$\mu\text{A}$
Standby Current	$I_{SB2}$	$V_{CC} = 5.0$	—	—	6	$\mu\text{A}$

**Power Supply Characteristics (TA = -55°C to +175°C)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCC Operating Current	$I_{CC1}$	Read at 400 KHz ( $V_{CC} = 5V$ )	—	—	2.0	mA
VCC Operating Current	$I_{CC2}$	Write at 400 KHz ( $V_{CC} = 5V$ )	—	—	3.0	mA
Standby Current	$I_{SB1}$	$V_{CC} = 2.5V$	—	—	60	$\mu\text{A}$
Standby Current	$I_{SB2}$	$V_{CC} = 5V$	—	—	120	$\mu\text{A}$

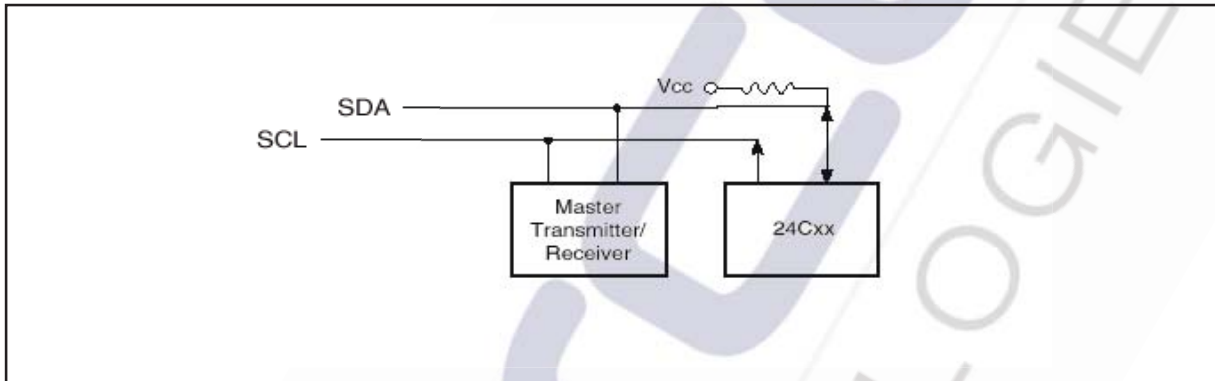


Figure 1. Typical System Bus Configuration

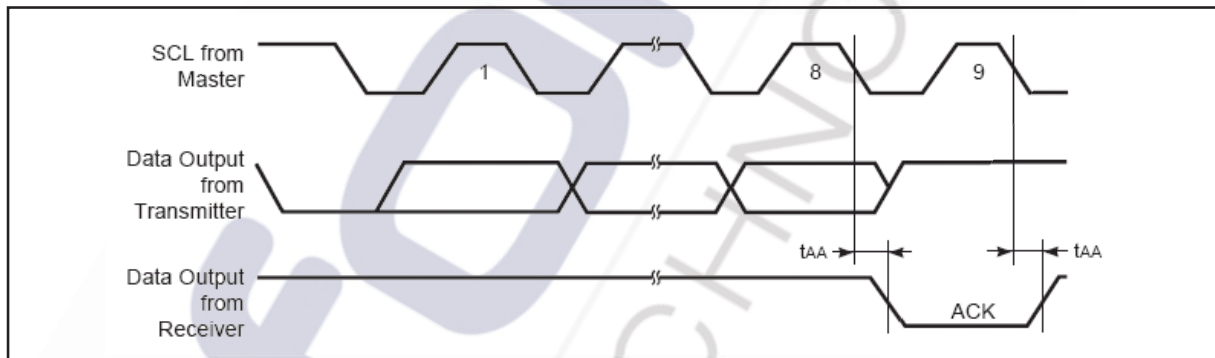


Figure 2. Output Acknowledge

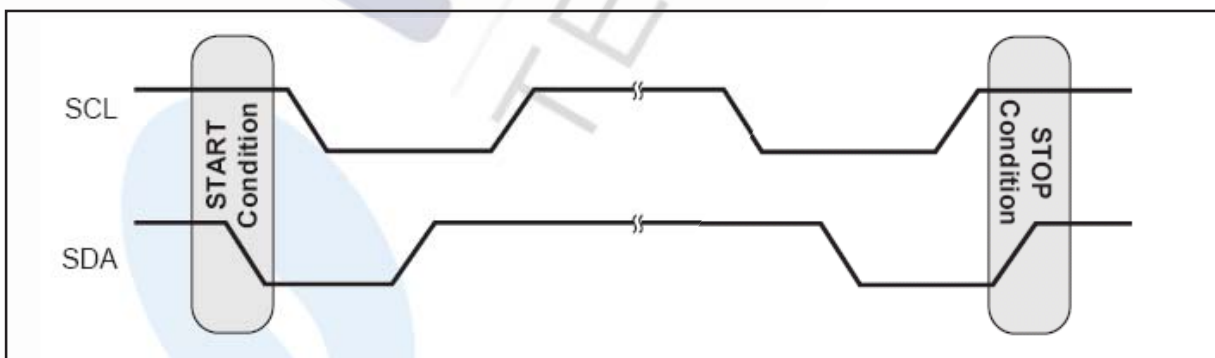


Figure 3. Start and Stop Conditions



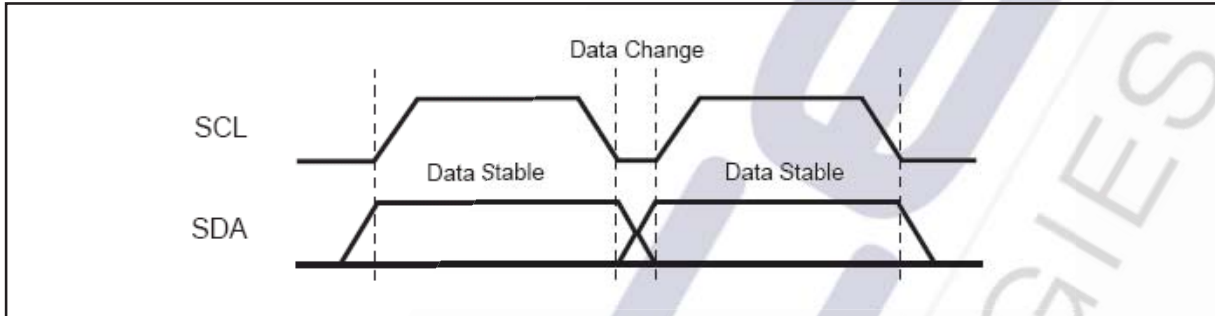


Figure 4. Data Validity Protocol

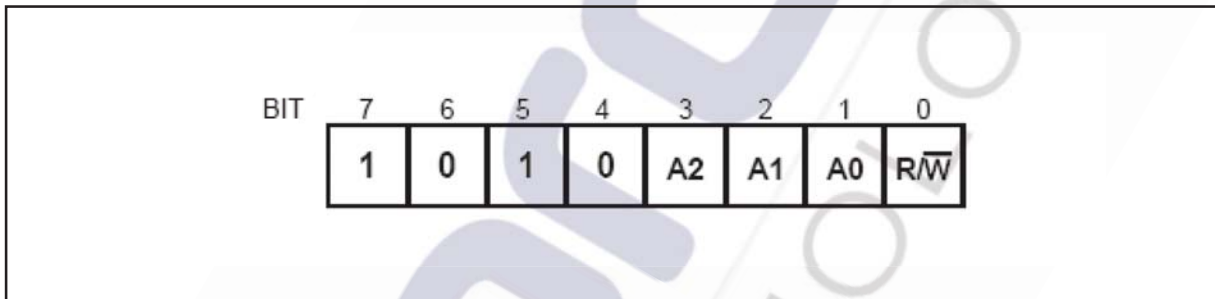


Figure 5. Slave Address

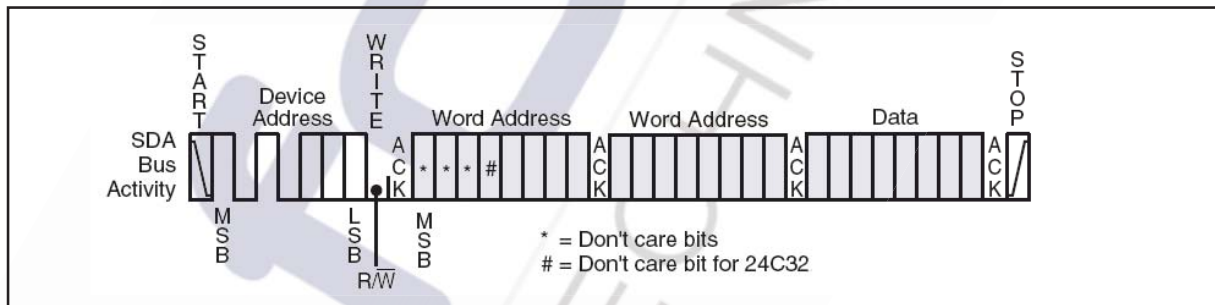


Figure 6. Byte Write

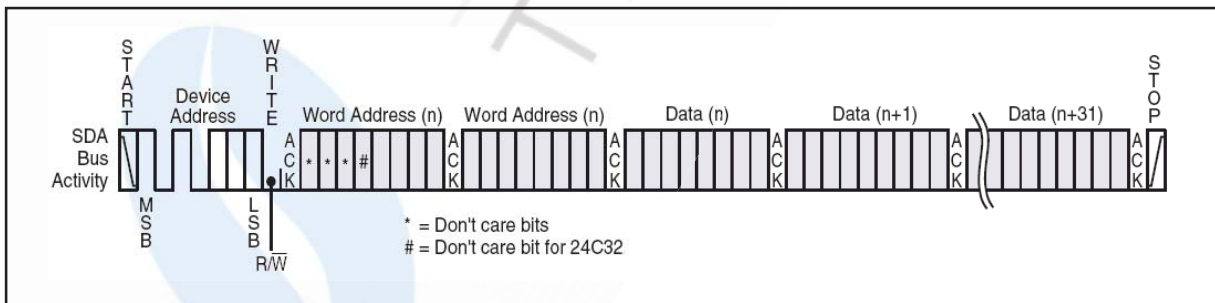


Figure 7. Page Write

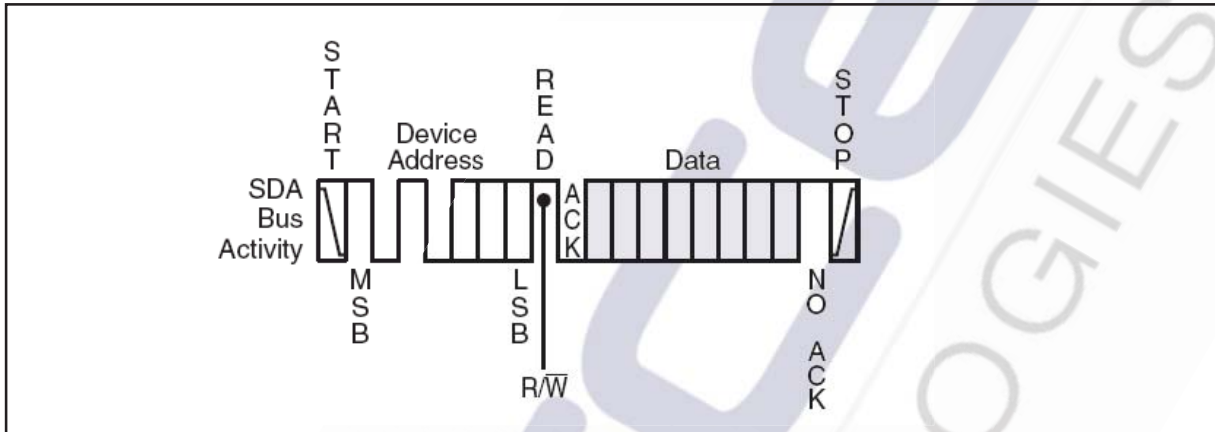


Figure 8. Current Address Read

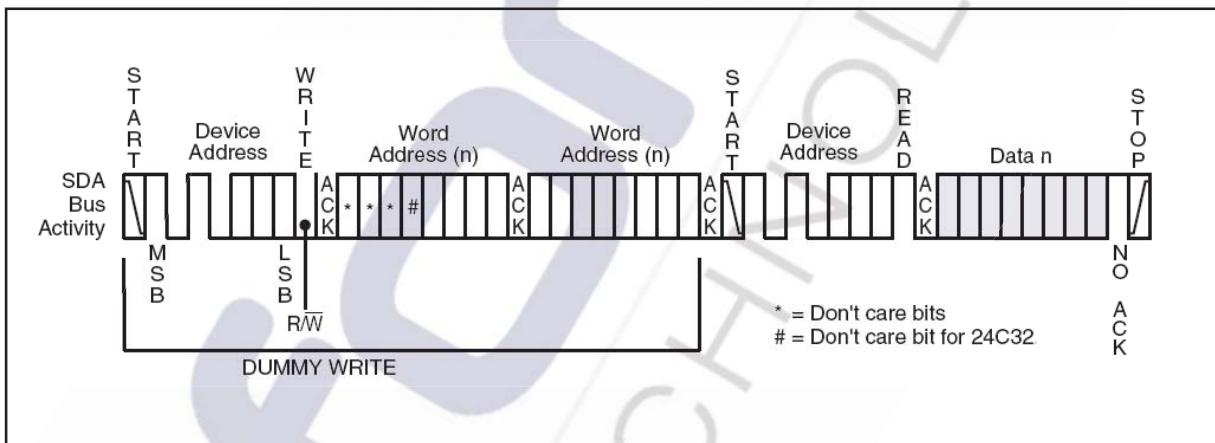


Figure 9. Random Address Read

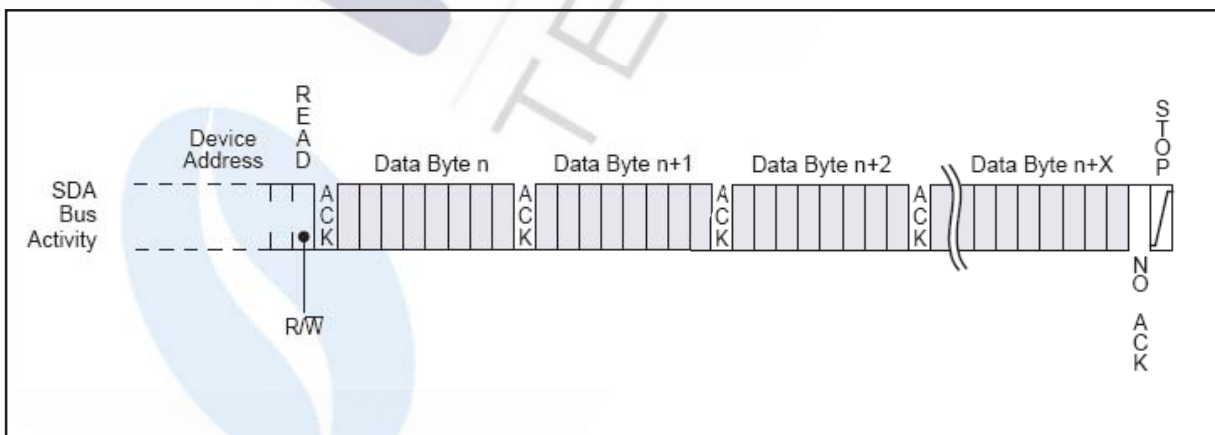


Figure 10. Sequential Read

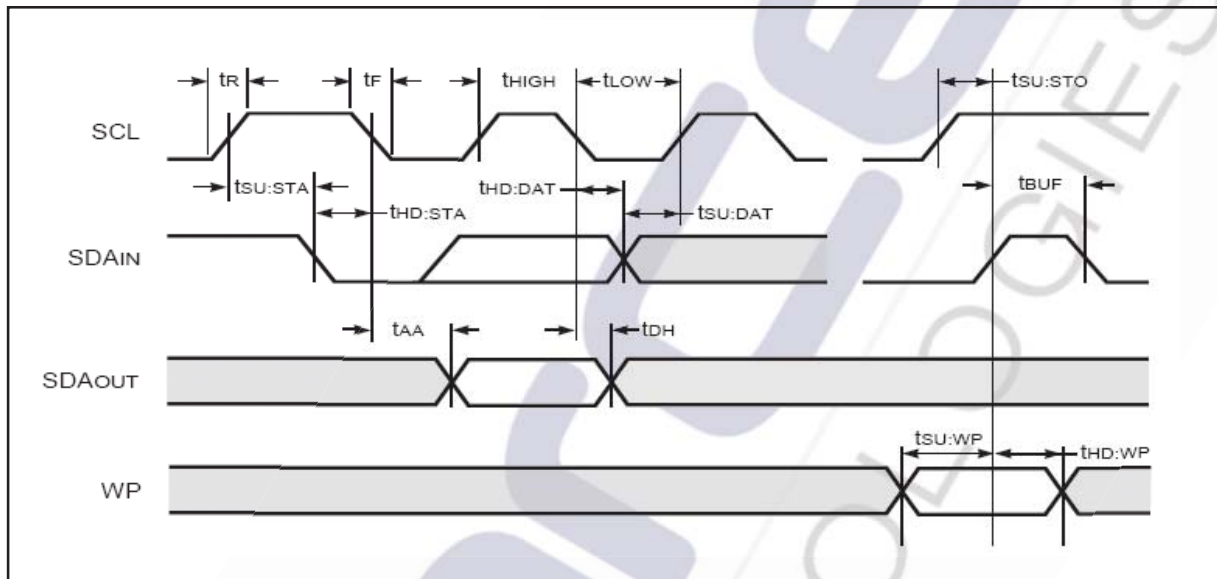


Figure 11. Bus Timing

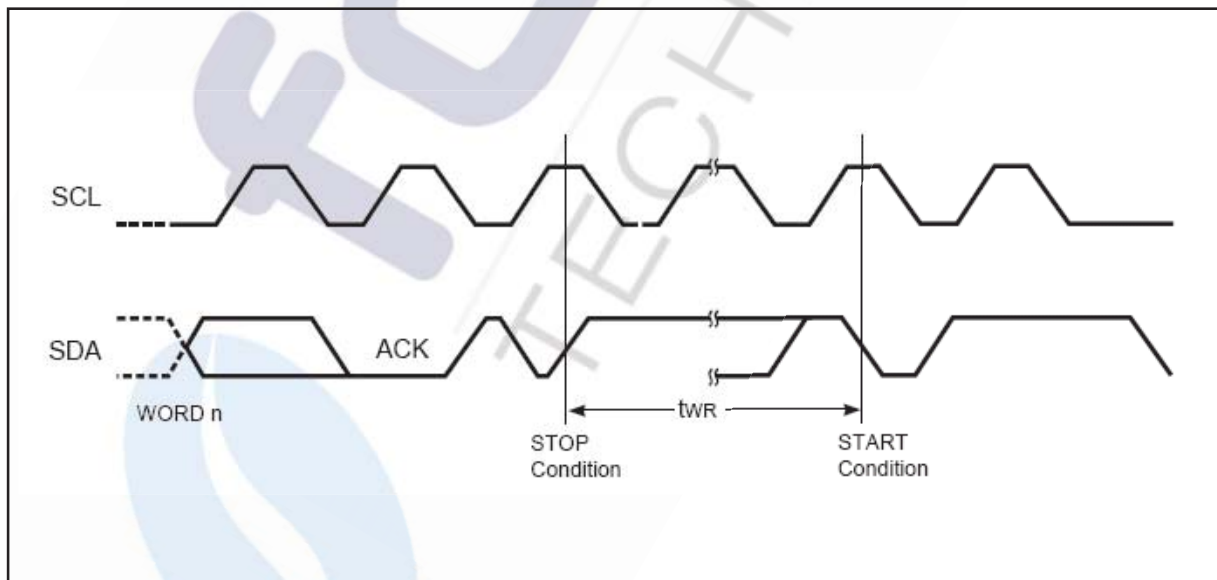


Figure 12. Write Cycle Timing

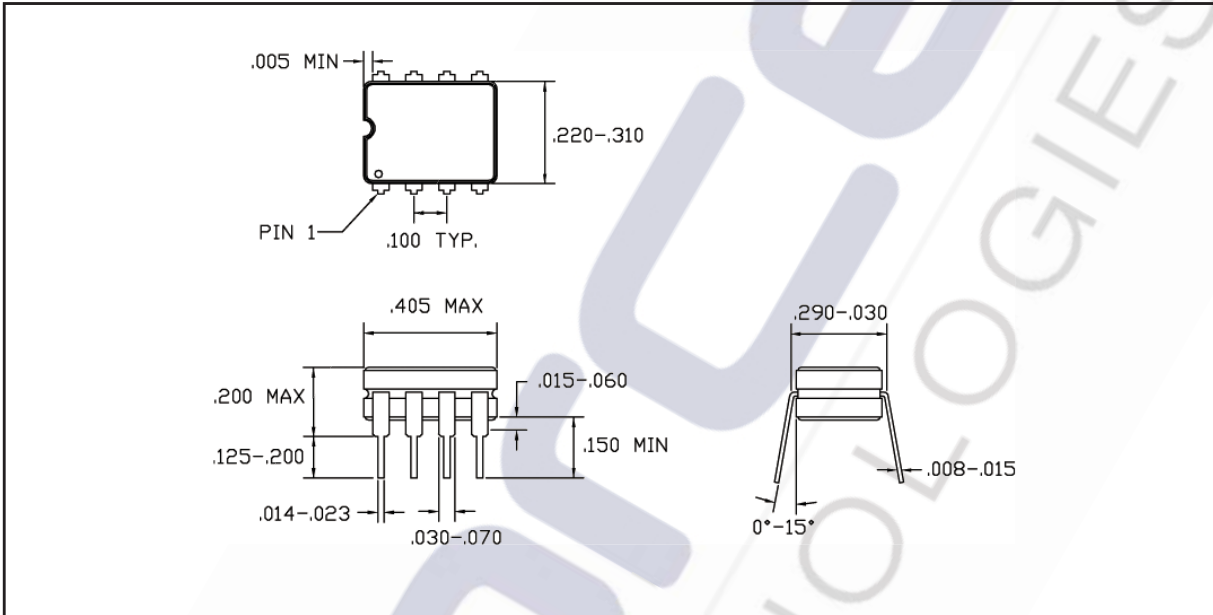


Figure 13. 8-pin PDIP and CDIP package outline

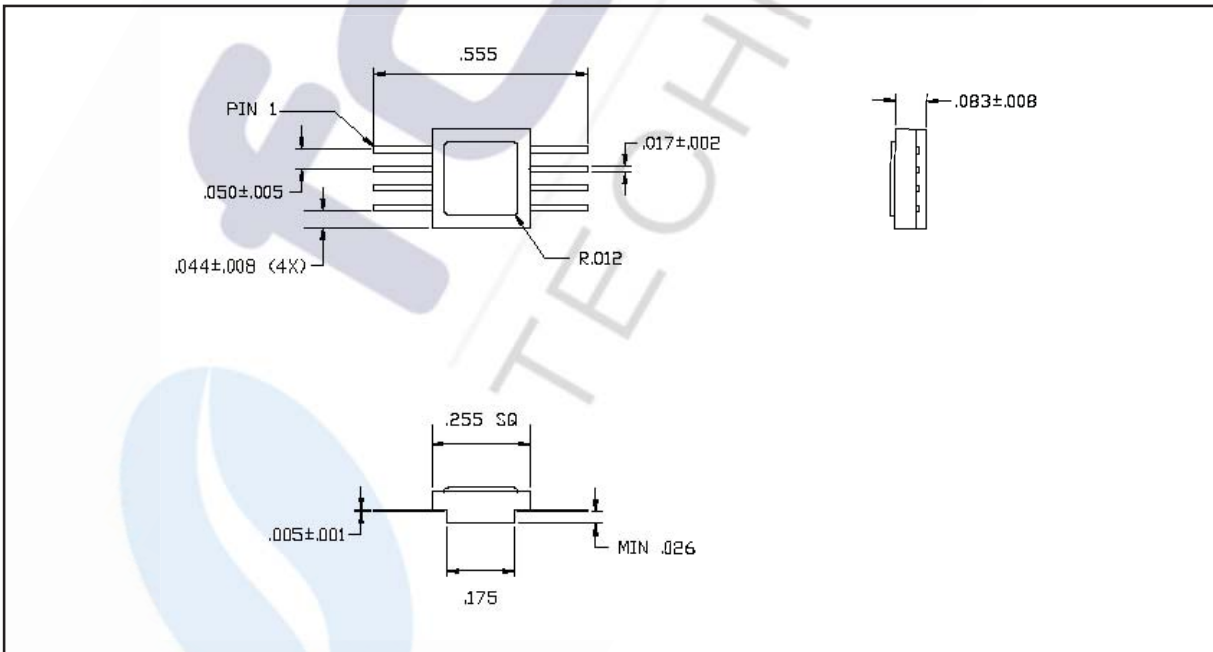


Figure 14. 8-pin Flatpack package outline

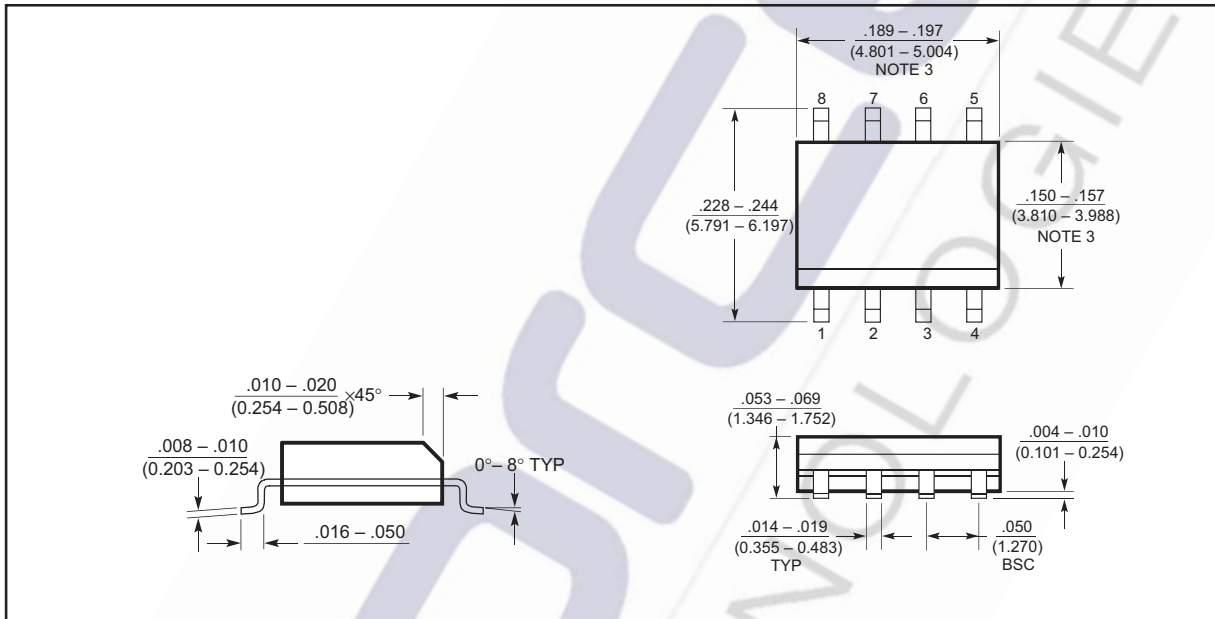


Figure 15. 8-pin SOIC package outline

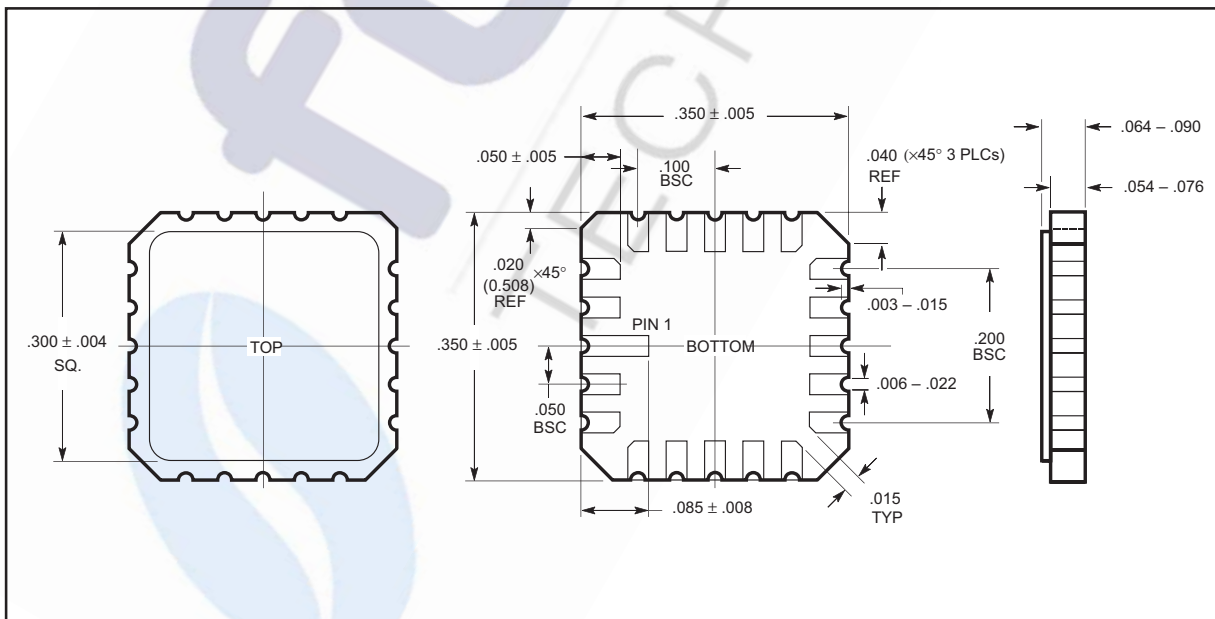


Figure 16. 20-pin LCC package outline



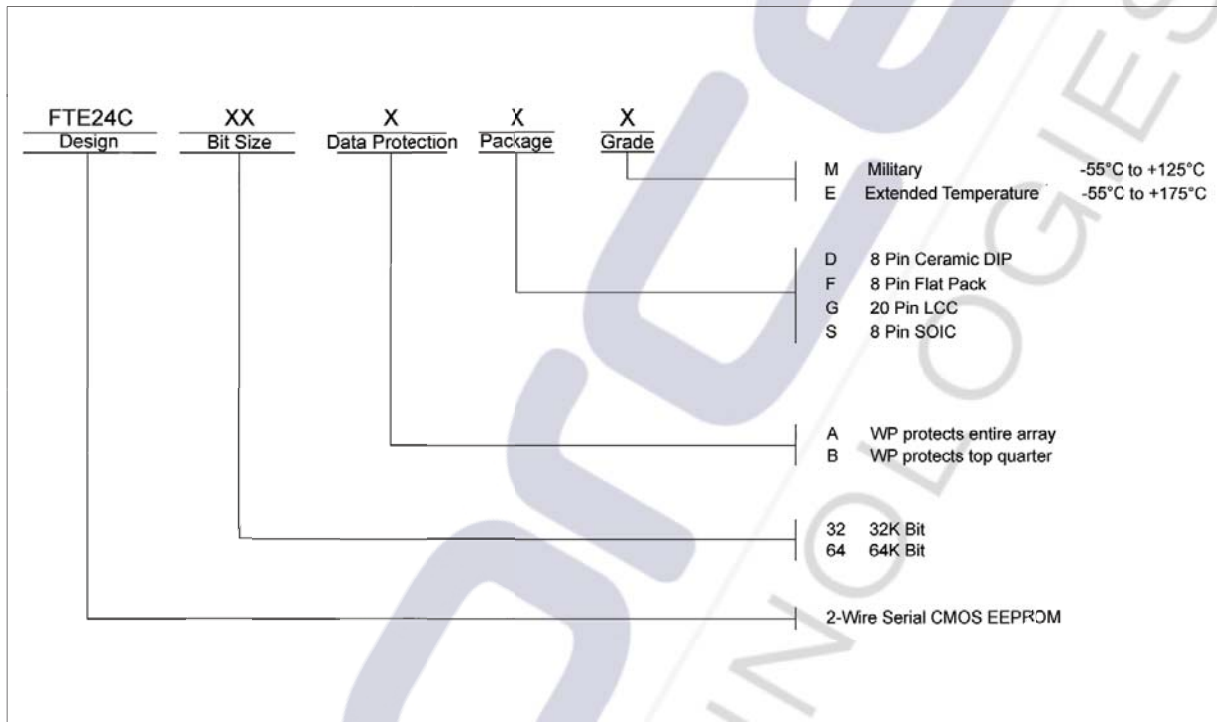


Figure 16. Order Information



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