FTS256S8N

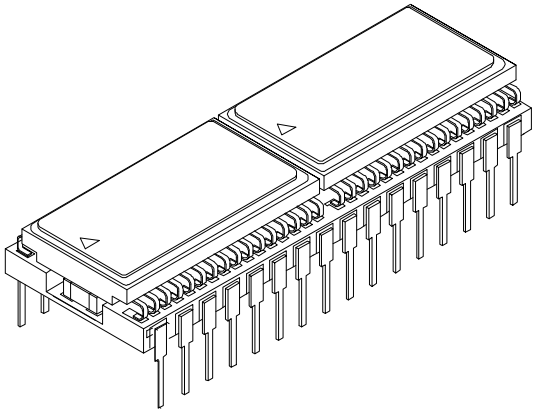
2 Megabit CMOS SRAM

DESCRIPTION:

The FTS256S8N is a Military 256K X 8 high-density, low-power static RAM module comprised of two ceramic 128K X 8 monolithic SRAM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

The FTS256S8N is available in a 600-mil-wide, 32-pin dual-in-line package that conforms to the same JEDEC standard pin configuration as the future four megabit monolithics.

The FTS256S8N operates from a single +5V supply and all input and output pins are completely TTL-compatible. The low standby power of the FTS256S8N make it ideal for battery-backed applications.



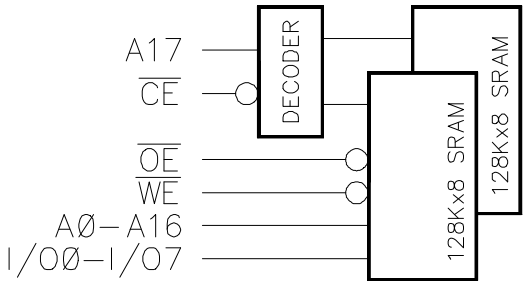
FEATURES:

- 262,144 by 8 bit configuration
- Access Times: 85*, 100, 120, 150ns
  - Faster Speeds Upon Request
- Low Power Dissipation:
  40 µW (typ.) standby
  375 mW (typ.) operating
- 2-Volt data retention
- Fully Static Operation - No clock or refresh required
- All inputs and outputs are TTL-compatible
- 600 mil, 32-pin JEDEC standard DIP pinout

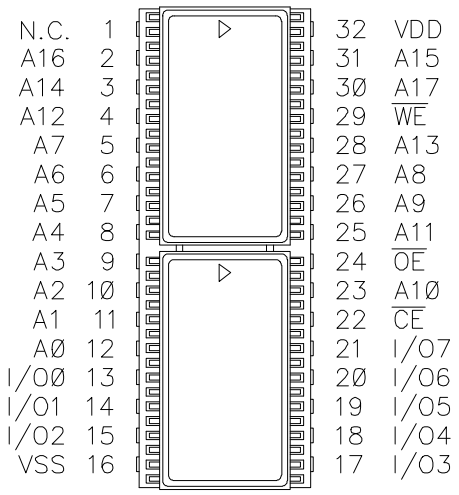
* Commercial Only.

PIN NAMES	
A0 - A17	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



RECOMMENDED OPERATING RANGE [1]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		$V_{DD}+0.3$	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

TRUTH TABLE						
Mode		$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected		H	X	X	HIGH-Z	Standby
Not Selected		X	X	X	HIGH-Z	Standby
D_{OUT} Disable		L	H	H	HIGH-Z	Active
Read		L	H	L	D_{OUT}	Active
Write		L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA		0.4	V

ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Max.	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	35	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	30		
C_{OE}	Output Enable	30		
$C_{I/O}$	Data Input/Output	35		

DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	TYP.	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-	-10	+10	-10	+10	-10	+10	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	30		50		50		60	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100%, I_{OUT} = 0mA	75		110		110		120	mA
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, $\overline{CE} \geq V_{DD}$ -0.2V	8		200		400		1000	µA
I_{SB2}	Standby Current	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IN}	3		6		6		6	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA	-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	-	2.4		2.4		2.4		V

* Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

DATA RETENTION CHARACTERISTICS										
Symbol	Parameter	Test Conditions	Typ. (†)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DR}$ -0.2V	-	2.0	5.5	2.0	5.5	2.0	5.5	V
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2.0V	4		90		170		700	µA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3.0V	4		100		200		800	µA
t_{CDR}	Chip Disable to Data Retention Time		-	0		0		0		ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing		5		5		5		ms

† Typical measurement made at +25°C, Cycle = min., V_{DD} = 5.0V.

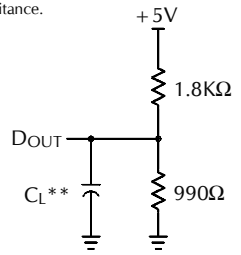
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	C_L	Parameters Measured
1	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}
2	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.

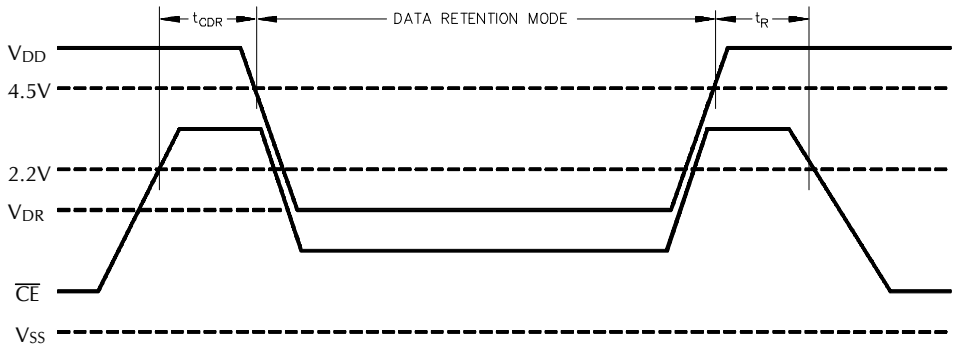


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	85		100		120		150		ns
2	t_{AA}	Address Access Time		85		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		40		45		50		60	ns
5	t_{OH}	Output Hold from Address Change	10		10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	5		5		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		0		0		0		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		45		45		50		60	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		30		30		35		45	ns

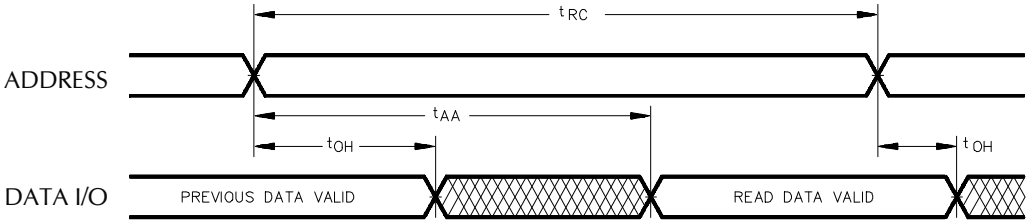
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]											
No.	Symbol	Parameter	85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	85		100		120		150		ns
11	t_{AW}	Address Valid to End of Write	80		90		105		115		ns
12	t_{CW}	Chip Enable to End of Write	80		90		105		115		ns
13	t_{DW}	Data to Write Time Overlap	35		35		40		50		ns
14	t_{DH}	Data Hold Time from Write Time	0		0		0		0		ns
15	t_{WP}	Write Pulse Width	55		65		75		85		ns
16	t_{AS}	Address Set-up Time ***	0		0		0		0		ns
17	t_{AH}	Address Hold Time	5		5		5		5		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		30		30		35		40	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns

*** Valid for both Read and Write Cycles.

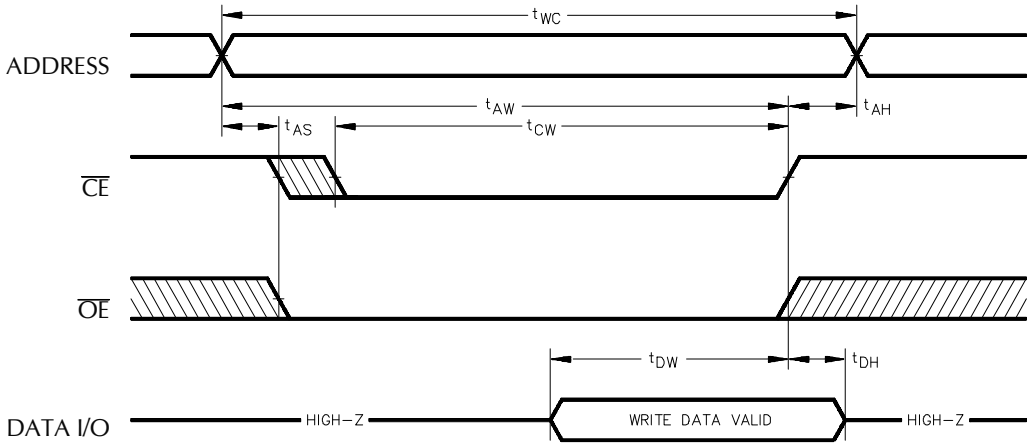
DATA RETENTION WAVEFORM



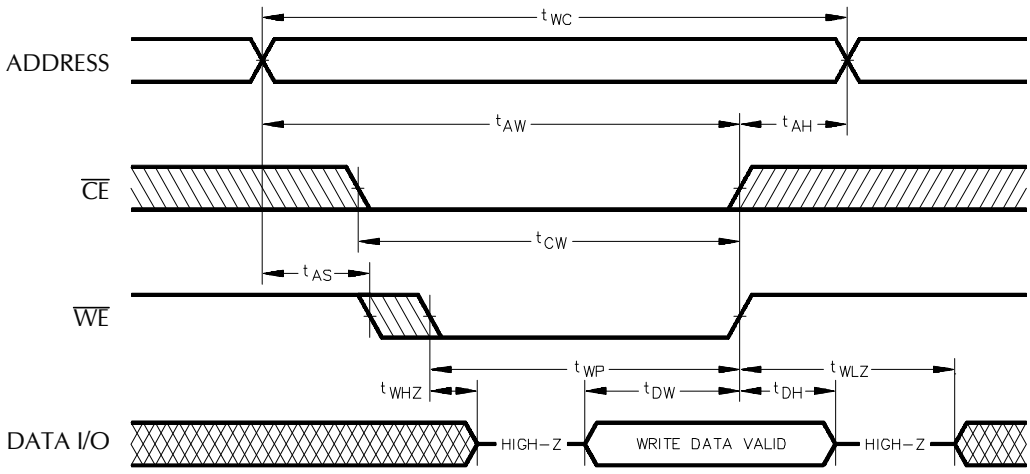
READ CYCLE 1: Address Controlled. WE is HIGH. CE and OE are LOW.



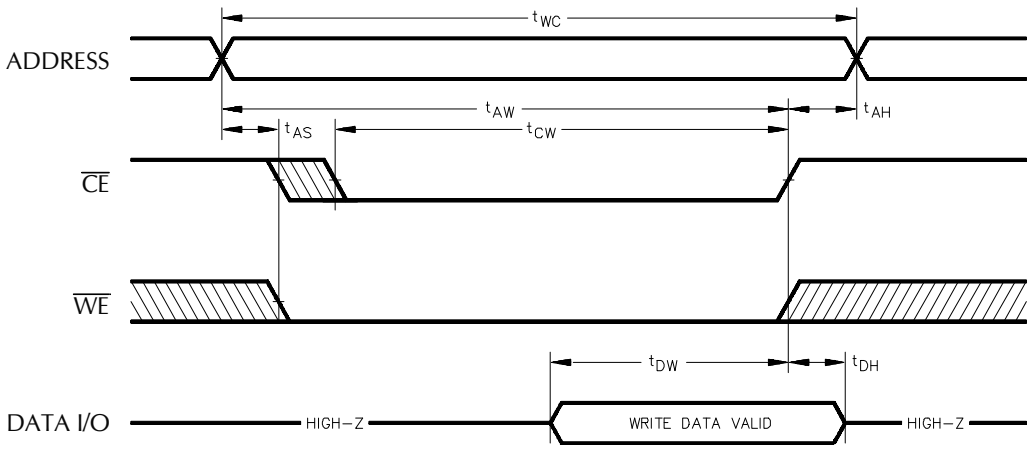
READ CYCLE 2: CE Controlled. WE is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.

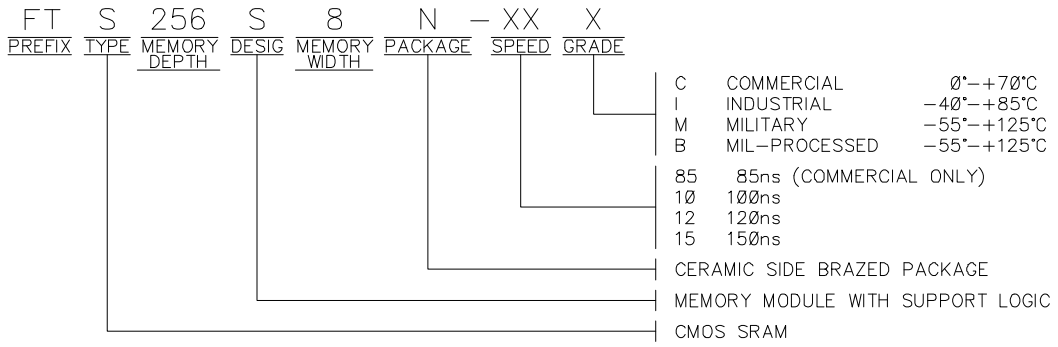


WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



WAVEFORM KEY

ORDERING INFORMATION



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

MECHANICAL DRAWING