

128K x 8 SRAM

Military Temp Screened Plastic(COTS)
HIGH SPEED

FEATURES

- Access times of 15, 20 and 25 ns
- Fast output enable (t_{AOE}) for cache applications
- Low active power
- Low standby power
- Fully static operation, no clock or refresh required
- TTL Compatible Inputs and Outputs
- Single +5V power supply
- Package in Industry-standard 32-pin SOJ

OPTIONS

- Timing
 - 15ns access
 - 20ns access
 - 25ns access

MARKING

- Package
 - Plastic SOJ* DJ
- Operating Temperature Ranges
 - Military (-55oC to +125oC) XT
 - Industrial (-40oC to +85oC) IT

GENERAL DESCRIPTION

The FTS5C1008 is a high speed, low power, 128K by 8-bit plastic (COTS) CMOS Static RAM. It is fabricated using high performance, CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15ns (Max) over the military and industrial temperature ranges.

When Chip Enable (CE\) is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down to 125mW (max) at CMOS input levels.

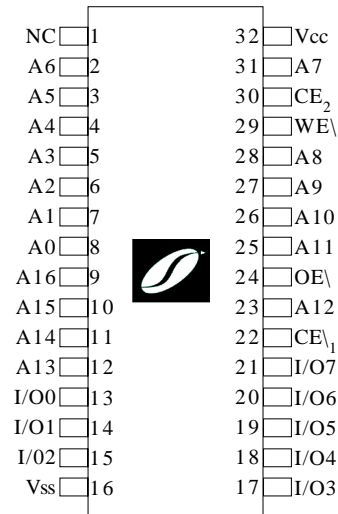
Easy memory expansion is provided by using asserted LOW CE\ and asserted HIGH CE₂, and asserted LOW write enable (WE\) controls both writing and reading of the memory.

The FTS5C1008 is pin-compatible with other 128K x 8 SRAM's in the SOJ package.

PIN ASSIGNMENT

(Top View)

32-Pin Plastic SOJ (DJ)



PIN FUNCTIONS

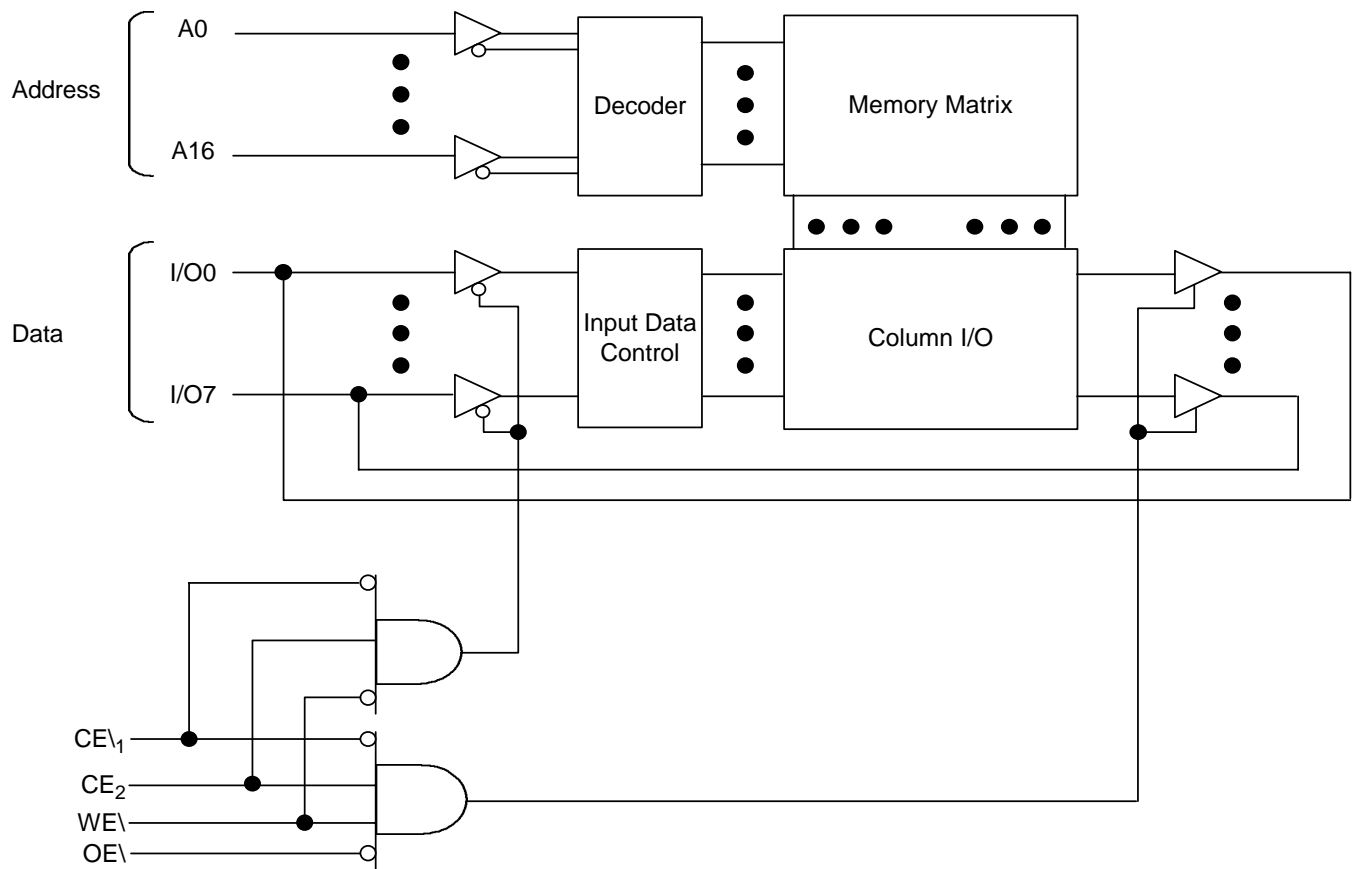
A0 - A16	Address Inputs
WE\	Write Enable
CE\ ₁ , CE ₂	Chip Enable
OE\	Output Enable
I/O ₀ - I/O ₇	Data Inputs/Outputs
V _{CC}	Power
V _{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Vcc Supply Relative to GND.....-0.5V to +7.0V
 Voltage on any pin Relative to GND.....-0.5V to Vcc +7.0V
 Storage Temperature-65°C to +150°C
 Ambient Temperature with Power Applied.....-55°C to +125°C
 Short Circuit Output Current.....260°C
 Power Dissipation.....1.0W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 (-55°C ≤ T_A ≤ +125°C or -40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	CONDITIONS	SYMBOL	-15		-20		-25		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Dynamic Operating Current	V _{CC} =MAX, I _{OUT} = 0mA, CE ₁ = V _{IL} and CE ₂ = V _{IH} , f = fmax	I _{CC1}		180		150		140	mA
TTL Standby Current - TTL Inputs	V _{CC} =MAX, V _{IN} = V _{IH} or V _{IL} , CE ₁ ≥ V _{IH} and CE ₂ ≥ V _{IL} , f = fmax	I _{SB1}		90		75		70	mA
CMOS Standby Current - CMOS Inputs	V _{CC} =MAX, CE ₁ ≥ V _{CC} - 0.2V, or CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V and V _{IN} ≤ 0.2V, f = 0	I _{SB2}		10		10		10	mA
Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	I _{LI}	-10	10	-10	10	-10	10	μA
Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} Output Disabled	I _{LO}	-10	10	-10	10	-10	10	μA
Output High Voltage	V _{CC} = MIN, I _{OH} = -4.0 mA	V _{OH}	2.4		2.4		2.4		V
Output Low Voltage	V _{CC} = MIN, I _{OL} = 8.0 mA	V _{OL}		0.4		0.4		0.4	V
Input High Voltage		V _{IH}	2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	V
Input Low Voltage		V _{IL}	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

PIN DESCRIPTIONS
A0 - A16: Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

CE₁: Chip Enable 1 Input

CE₁ is asserted LOW to read from or write to the device. If Chip Enable 1 is deasserted, the device is deselected and is in standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

CE₂: Chip Enable 2 Input

CE₂ is asserted HIGH to read from or write to the device. If Chip Enable 2 is deasserted, the device is deselected and is in standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

OE₁: Output Enable Input

The Output Enable Input is asserted LOW. If asserted LOW while CE₁ is asserted (LOW) and CE₂ is asserted (HIGH) and WE₁ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when OE₁ is deasserted.

WE₁: Write Enable Input

The Write Enable input is asserted LOW and controls read and write operations. When CE₁ and WE₁ are both asserted (LOW) and CE₂ is asserted (HIGH) input data present on the I/O pins will be written into the selected memory location.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (-55°C ≤ T_A ≤ +125°C or -40°C to +85°C; V_{CC} = 5V ± 10%)

DESCRIPTION	SYMBOL ¹	-15		-20		-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
Read Cycle Time	t _{RC}	15		20		25		ns
Address Access Time	t _{AA}		15		20		25	ns
Chip Enable Access Time	t _{ACE}		15		20		25	ns
Output Hold from Address Change	t _{OH}	3		3		3		ns
Chip Enable to Output in Low-Z	t _{LZCE}	3		3		3		ns
Chip Disable to Output in High-Z	t _{HZCE}		7		8		10	ns
Output Enable Access Time	t _{AOE}		7		7		10	ns
Output Enable to Output in Low-Z	t _{LZOE}	0		0		0		ns
Output Disable to Output in High-Z	t _{HZOE}		7		8		10	ns
WRITE CYCLE								
Write Cycle Time	t _{WC}	15		20		25		ns
Chip Enable to End of Write	t _{CW}	12		15		20		ns
Address Valid to End of Write	t _{AW}	12		15		20		ns
Address Set-up Time	t _{AS}	0		0		0		ns
Address Hold from End of Write	t _{AH}	0		0		0		ns
Write Pulse Width (OE \ ≥ V _{IH})	t _{WP}	12		15		20		ns
Data Set-up Time	t _{DS}	8		10		15		ns
Data Hold Time	t _{DH}	0		0		0		ns
Write Disable to Output in Low-Z	t _{LZWE}	5		5		5		ns
Write Enable to Output in High-Z	t _{HZWE}		7		9		10	ns

NOTE: 1. t_{LZCE}, t_{LZWE}, t_{HZCE}, t_{LZOE}, and t_{HZOE} are simulated values.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

PARAMETER	CONDITION	SYMBOL	MAX	UNIT
Input Capacitance	$V_{IN} = 0V$	C_{IN}	6	pF
Output Capacitance	$V_{OUT} = 0V$	C_{OUT}	8	pF

AC TEST CONDITIONS

Input Pulse Levels.....	GND to 3.0V
Input Rise and Fall Times.....	3ns
Input Timing Reference Levels.....	1.5V
Output Reference Levels.....	1.5V
Output Load.....	See Figure 1

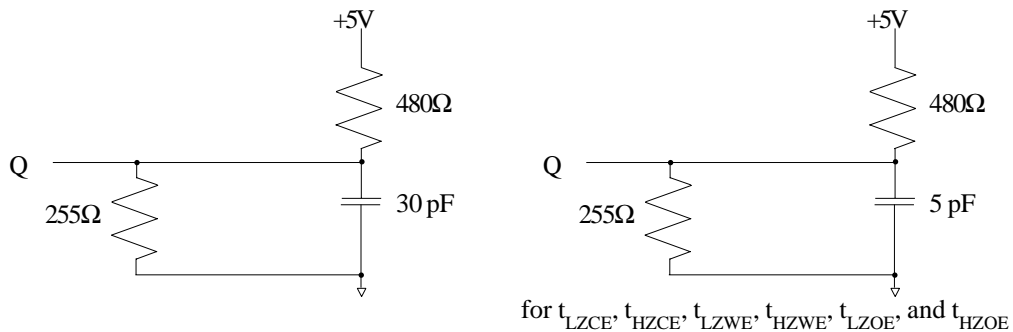
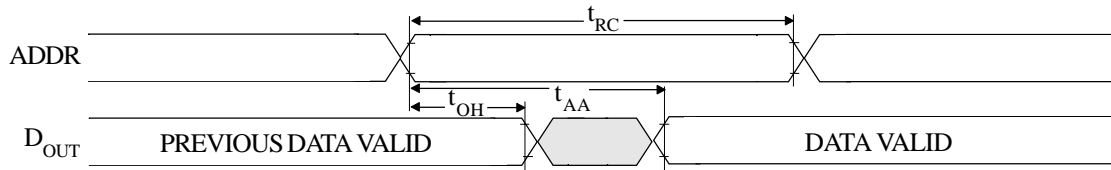


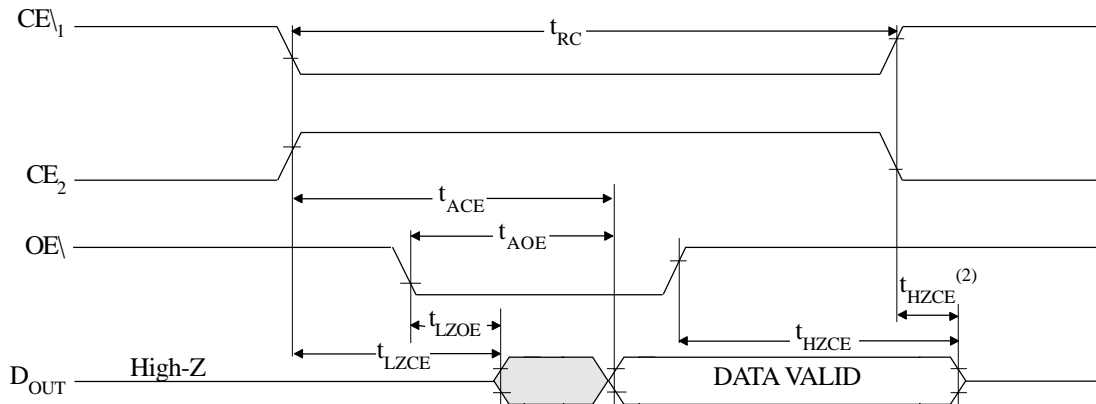
Fig. 1 OUTPUT LOAD EQUIVALENT

READ CYCLE TIMING 1⁽¹⁾



NOTE: 1. CE\ is HIGH for READ cycle.

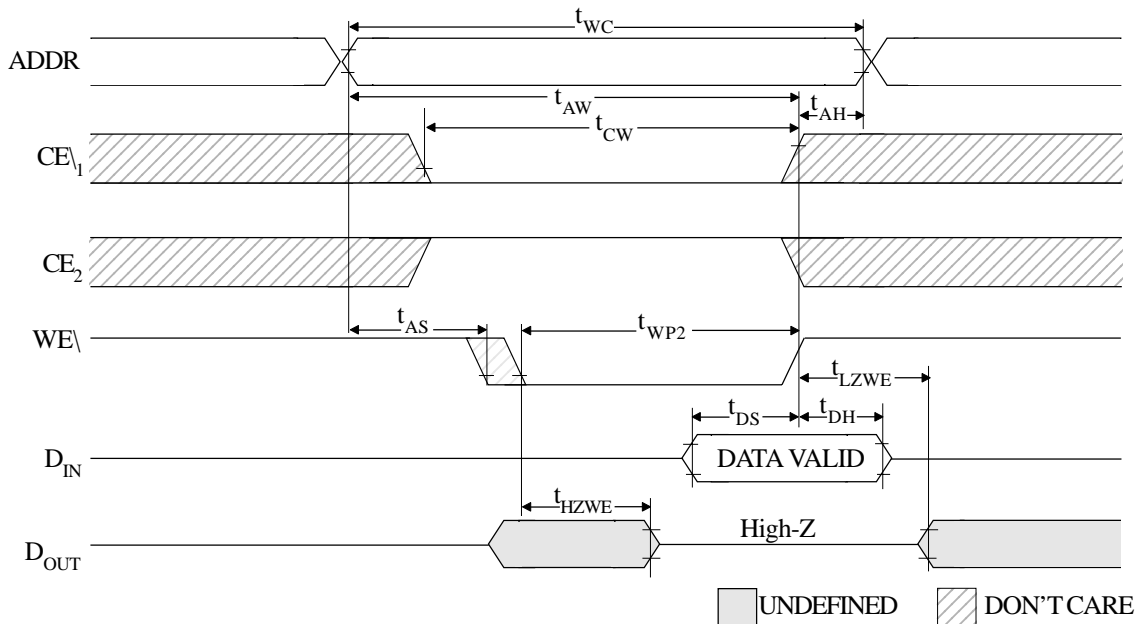
READ CYCLE TIMING 2⁽¹⁾



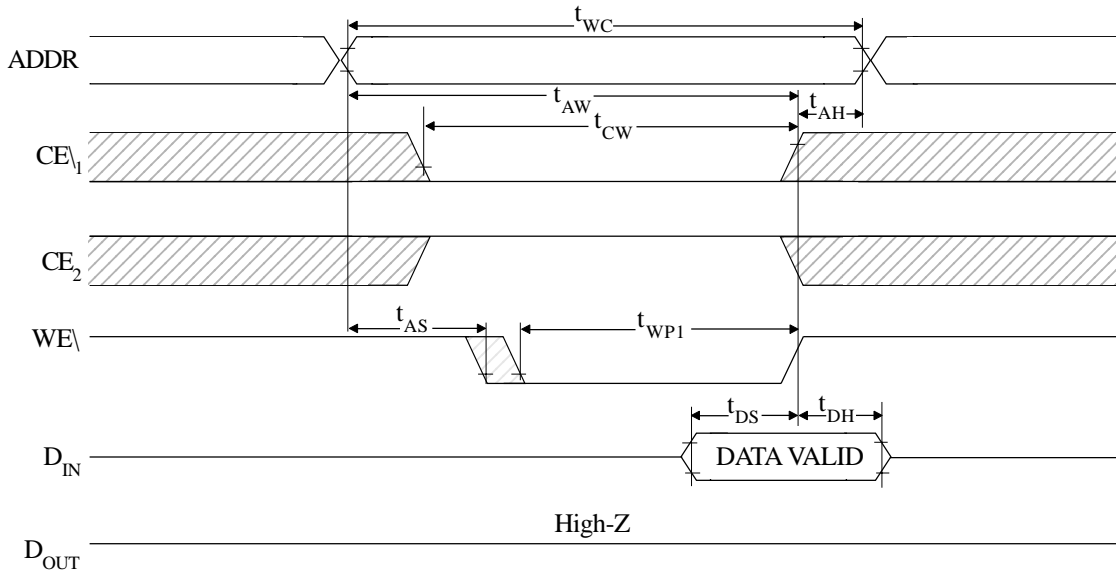
NOTES: 1. CE\ is HIGH for READ cycle.

2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} .

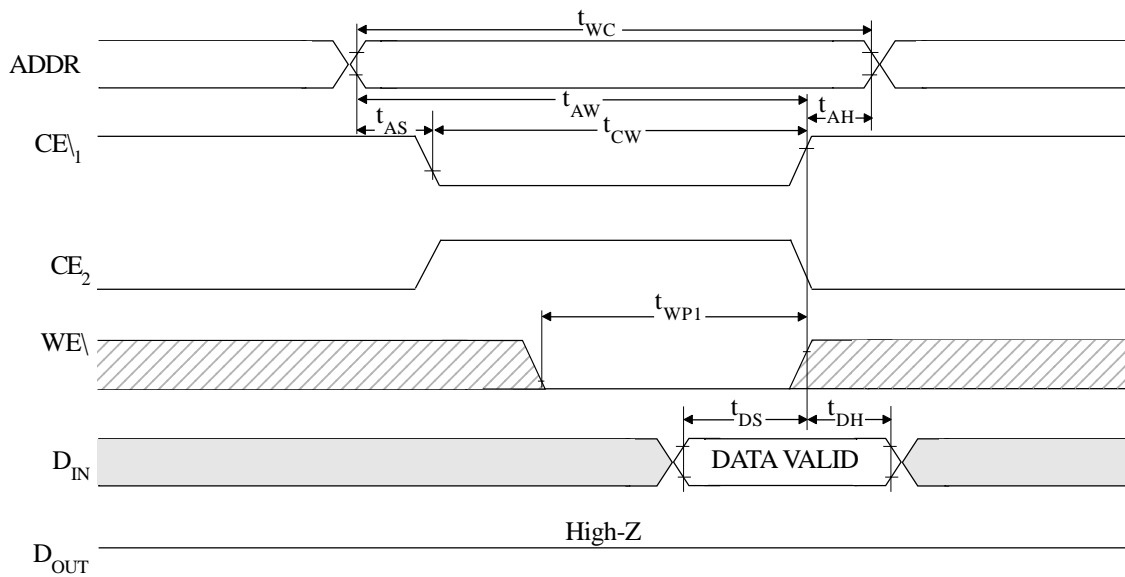
WRITE CYCLE TIMING (WE\ CONTROLLED, OE\ = LOW)



WRITE CYCLE TIMING (CE₁ CONTROLLED, OE = LOW)



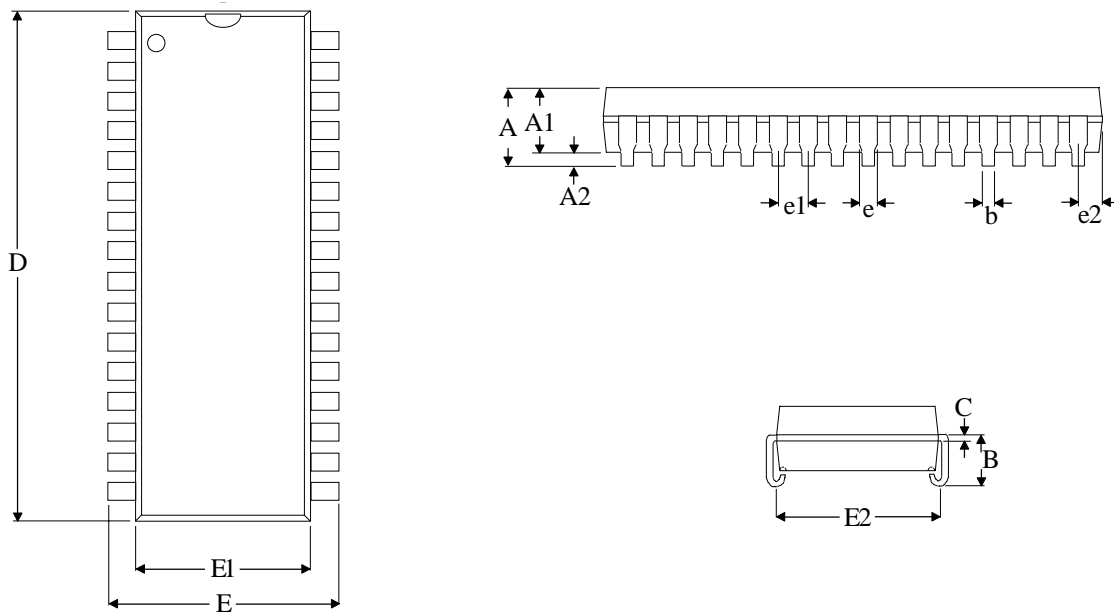
WRITE CYCLE TIMING (CE₂ CONTROLLED, OE = LOW)



□ UNDEFINED ▨ DON'T CARE

MECHANICAL DEFINITION*

(Package Designator DJ)



SYMBOL	SPECIFICATIONS	
	MIN	MAX
A	0.140 BSC	
A1	0.105	0.115
A2	0.027 TYP	
B	0.082	---
b	0.018 TYP	
C	0.010 TYP	
D	0.820	0.880
E	0.430	0.445
E1	0.395	0.405
E2	0.360	0.380
e	0.025	0.032
e1	0.050 TYP	
e2	---	0.045

* All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: FTS5C1008DJ-25XT

Device Number	Package Type	Speed ns	Process
FTS5C1008	DJ	-15	*
FTS5C1008	DJ	-20	*
FTS5C1008	DJ	-25	*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range

-40oC to +85oC

XT = Extended Temperature Range

-55oC to +125oC



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